

ITCH for High Frequency Trading (HFT) with FPGA

ITCH Protocol

ITCH is a direct data-feed protocol for accessing market data and is used for information exchange. It helps clients to track the status of each of their orders whether they've been executed or canceled from the beginning of order placement. The targeted board platform for our implementation is Xilinx Virtex UltraScale+ Board with part of VU9P FPGA. Here are some details on implementation of its decoder.

Specifications:

Minimum Operating Frequency	350 MHz
Throughput	~7GBps
Maximum Latency	14 ns
Number of Input ports	3
Number of Output ports	221
Bit-Width of Input data	776
Number of Message Types decoded	16
Byte Ordering	Big Endian

Decoded Message Types:

- System Event
- Stock Trading Action
- Order Book Directory
- Add Order Mpid
- Add Order No Mpid
- Order Executed
- Order Delete
- Order Executed with Price
- Order Cancel
- Order Book Flush
- Order Replace
- Trade
- Cross Trade
- Broken Trade
- NOII
- MOII

Design Structure:

Similar to ouch decoder, itch decoder is also divided into three stages. First stage identifies the message types, second extracts the direct values available in input data for a given message type and the third stage decodes the relevant information from the second stage as per the itch specification. Here too the latency of output corresponds to the different stages.

Testing Methodology:

For testing we first designed input encoded stimulus such that every output(221 ports) of the itch engine is triggered in a way that is easier to analyze. Upon close inspection of input and output mapping, the itch engine design worked as expected.

Implementation details:

We implemented such decoder/encoder & itch decoder for building tick to trade system in FPGA. These implementations are optimized for low latency which is around 15 ns or less. All engines are implemented on VHDL using Xilinx VIVADO as a simulator.

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