OUCH for High Frequency Trading (HFT) with FPGA

OUCH protocol

Ouch is the low level native protocol for connecting to NASDAQ. It allows NASDAQ participants to enter, replace & cancel orders and receive executions. The protocol is composed of logical messages passed between OUCH host and client application. The targeted board platform for our implementation is Xilinx Virtex UltraScale+ Board with part of VU9P FPGA. Here are some details of OUCH encoder and decoder engines.

OUCH Decoder:

Ouch decoder receives the outbound messages from NASDAQ through TCP and decodes it making it accessible for further processing with order book and custom trading algorithm. Here are some details on its implementation.

Specifications:

Minimum Operating Frequency	300 MHz
Throughput	~5GBps
Maximum Latency	16 ns
Number of Input ports	3
Number of Output ports	265
Bit-Width of Input data	640
Number of Message Types decoded	15
Byte Ordering	Big Endian

Decoded Message Types:

- System Event
- Accepted
- Replaced
- Cancelled Order
- Aiq Cancelled
- Order Executed
- Broken Trade
- Order Executed with Reference Price
- Trade Correction
- Rejected Order
- Cancel Pending
- Cancel Reject
- Order Priority Update
- Order Modified
- Trade Now

Design Structure:

The design is separated in three stages. In the first stage we identify all 15 message types. In the second stage we decode the information that is directly available for a given message type such as event codes, order tokens, share, stock price etc. In the third stage we decode what values from the second stage mean. for eg. start or end of day, display attributes, bbo weight indicator, liquidity flags etc.

The latency we get directly corresponds to stages of the design.

Testing Methodology:

For testing we provided encoded messages as stimulus to decoder. Stimulus data were manually designed such that every possible data output port (265 of them) were to be triggered. Upon close inspection of each port, we got all output as expected.

Ouch Encoder:

Ouch Encoder encodes the data to be sent as an inbound message from participant to ouch host. Here are some details of its implementation.

Specifications:

Minimum Operating Frequency	300 MHz
Throughput	~ 3.6GBps
Maximum Latency	13 ns
Number of Input ports	78
Number of Output ports	1
Bit-Width of Output data	392
Number of Message Types decoded	5
Byte Ordering	Big Endian

Encoded Message Types:

- Enter Order
- Replace Order
- Cancel Order
- Modify Order
- Trade Now

Testing Methodology:

For testing we stimulated each of 75 inputs one by one and looked at each output whether it fits ouch protocol specifications or not.

Implementation details:

We implemented ouch decoder/encoder & itch decoder for building tick to trade system in FPGA. These implementations are optimized for low latency which is around 15 ns or less. All engines are implemented on VHDL using Xilinx VIVADO as a simulator.

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