Auto Contrast Enhancement (ACE)

V1.0

Introduction

The IP core produces the low-contrast enhanced output stream by histogram analysis of the input stream without loss of image details. The IP follows AXI4 protocol allowing easy IP integration with the user's design.

IP core has AXI4 interface ports for stream, memory and control.

Features

- Generates contrast-enhanced output.
- Configurable parameters such as resolution, gray level, enhance mode(0 - original unenhanced output, 1 - contrast-enhanced output)
- Supports a maximum of 1920x1080, resolution with 1 pixel per clock,
- AXI4-Lite control interface,
- AXI4-Stream interface for input and output video,
- AXI4-MM interface for reading stream data from memory
- Supports 24-bit RGB input and output.

Applications

- Thermal Imaging
- Bio-Medical Imaging
- Machine Vision

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000
Supported User Interfaces	AXI4-MM, AXI4-Lite, AXI4-Stream
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

Overview

The Auto Contrast Enhancement (ACE) IP core implements a histogram analysis mechanism to enhance the output. So that, IP can take any sort of RGB image input and then automatically enhances those images which require contrast enhancement. In other words, the IP core selectively enhances the low contrast images only. The output will be not changed if already enhanced image input is given. So, the IP core is particularly very useful for enhancing low contrast grayscale streams, such as camera sensor image, thermal image, bio-medical images etc. The IP has internally sub-cores for doing histogram analysis and contrast enhancement parallelly.

The IP supports a maximum of 1920x1080 video resolution. The IP has AXI4-compliant input and output stream interfaces. These interfaces support a 24-bit RGB format. The IP allows the user to get original stream output (not enhanced) or enhanced output, which can be done by setting mode 0 or 1 respectively from the software application. The IP also has an AXI4-MM interface, which is used for histogram analysis of an image frame.

Port Description

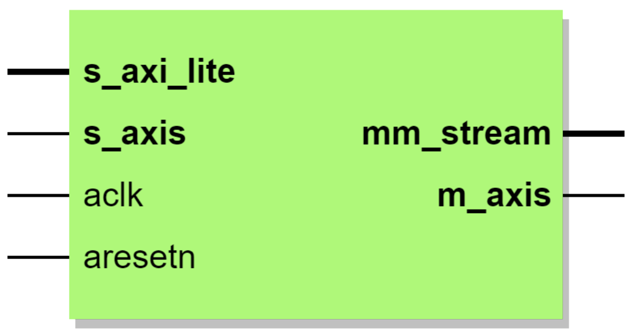


Figure 1. Auto Contrast Enhancement (ACE) IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow easy integration and communication with other IPs or systems. The ACE core ports are described by the following interfaces.

1. Clock, Reset and Interrupt signal Interface

These signals are summarized in the following table.

Signal Name	Width	Direction	Description
aclk	1	IN	Core clock for both AXI4-Stream as well as AXI4-Lite Interface
aresetn	1	IN	Core ap_clk synchronous active low reset

Table 2. Clock, Reset and Interrupt Signal Interface Description

2. Video Interface

The IP has two data interfaces *s_axis* and *m_axis* that implement the AXI4-Stream interface protocol. These interfaces are used to get input as well as output stream data respectively.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Signal Name	Width	Direction	Description
AXI4-Stream Input Signals			
s_axis_tdata	24	OUT	Input video Data
s_axis_tvalid	1	OUT	Input valid
s_axis_tready	1	IN	Input ready
s_axis_tuser	1	OUT	Input video start of frame
s_axis_tlast	1	OUT	Input video end of line
s_axis_tstrb	3	OUT	Input video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
s_axis_tkeep	3	OUT	Input video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
s_axis_tid	1	OUT	Input video data identifier
s_axis_tdest	1	OUT	Input video data routing information
AXI4-Stream Output Signals			
m_axis_tdata	24	OUT	Output video Data
m_axis_tvalid	1	OUT	Output valid
m_axis_tready	1	IN	Output ready
m_axis_tuser	1	OUT	Output video start of frame
m_axis_tlast	1	OUT	Output video end of line

m_axis_tstrb	3	OUT	Output video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
m_axis_tkeep	3	OUT	Output video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
m_axis_tid	1	OUT	Output video data identifier
m_axis_tdest	1	OUT	Output video data routing information

Table 3. AXI4-Stream Signal Names and Descriptions

Both streaming interfaces run at *aclk*.

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface. This allows users to configure or control the IP dynamically. This interface will be connected to Zynq PS or Microblaze.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready. INdicates DMA ready to accept the wire address.
s_axi_lite_awaddr	6	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe

s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel. Indicates results of the write transfer
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready. This indicates the target is ready to receive a response.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready. Indicates DMA is ready to accept the read address.
s_axi_lite_araddr	6	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready. INdicates target is ready to accept the read data.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response. INdicates results of the read transfer.

Table 4. AXI4-Lite Interface Signal Names and Description

This interface also runs at the *aclk* clock.

4. Memory Interface

The IP consists of an AXI4-MM interface. This interface is used for histogram analysis to read the input image data from the buffer.
The name and the description is given in the following table.

Signal Name	Width	Direction	Description
mm_stream	-	-	Input stream reading from buffer. Follow Ref. 1 for more information about AXI4 Signals.

Table 5. Memory-mapped AXI4 interface and Description

Register Space

The IP has a number of registers. These can be accessed by their offset address. Instead of using software API, these registers can eventually be used to configure the IP. As IP core is created with sub-blocks inside, the registers are programmed to configure sub-blocks parameters.

The register name, address and description are given below.

BASEADDR Offset (Hex)	Register Name	Type	Description
0x00	Control Signals	R/W	Bit 0: ap_start Bit 1: ap_done Bit 2: ap_idle Bit 3: ap_ready Bit 7: auto_restart Others: Reserved
0x04	Global Interrupt Enable Register	R/W	Bit 0: Global Interrupt Enable Others: reserved
0x08	IP Interrupt Enable Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x0C	IP Interrupt Status Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x10	StartH	R/W	Start histogram sub-block
0x18	StartC	R/W	Start contrast enhancement sub-block
0x20	Mode	R/W	Contrast enhancement mode
0x28	GrayLevel	R/W	Gray level value
0x30	Active Height	R/W	Number of Active Lines Per Frame
0x38	Active Width	R/W	Number of active pixels per scanline
0x40	Addr	R/W	Assign 32-bit address value

Table 6. IP Register Names, Offset Addresses and Descriptions

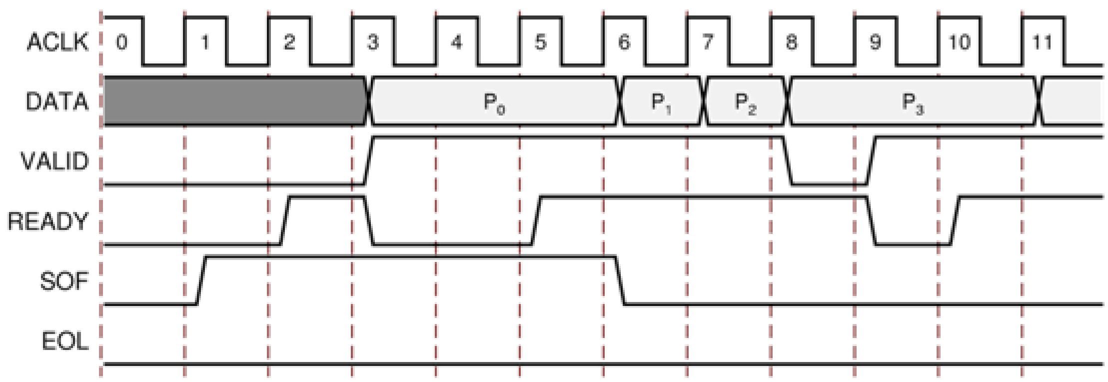
Video Data

The core generates RGB video data with 1 pixel per clock and 8-bits per component through the *m_axis* port.

Figure 2. Single Pixel Per Clock, 8-bits per component RGB Video Data Format

Note: Currently IP generates pixel data with 8-bit per color component. However, the IP will be updated to support 10-bit, 12-bit and 16-bit in the future version of IP.

Data Flow



Ref. Xilinx’s PG103

Figure 3. AXI4-Stream Data flow mechanism

The flow of data follows the AXI4-Stream protocol. *tvalid*, *tready*, *tuser* (SOF) and *tlast* (EOL) are responsible signals for the data flow. These signals are called AXI4-stream handshaking signals. The data is carried out by *tdata* line.

The IP core has bidirectional data throttling. The data flow takes place from master to slave through this IP core. To receive the data from the master, this IP core asserts *tready* signal HIGH but the master also needs to assert its *tvalid* signal HIGH. On the contrary, for the flow of the valid data from ACE IP to its slave, the IP asserts *tvalid* HIGH. Meantime, the slave must also assert its *tready* HIGH and then the actual flow of data takes place. This all means that the flow of data takes place as long as the master produces valid data and the slave is ready to receive data.

For a complete transfer of a frame, the SOF signal goes high, which indicates the beginning of the frame. During this moment, *tready* and *tvalid* must be at HIGH state to begin the flow of valid data from this IP to slave IP. EOL is asserted HIGH when the transfer of pixels per scanline is completed.

Designing with the ACE IP core

The design with the core has been summarized in the following picture.

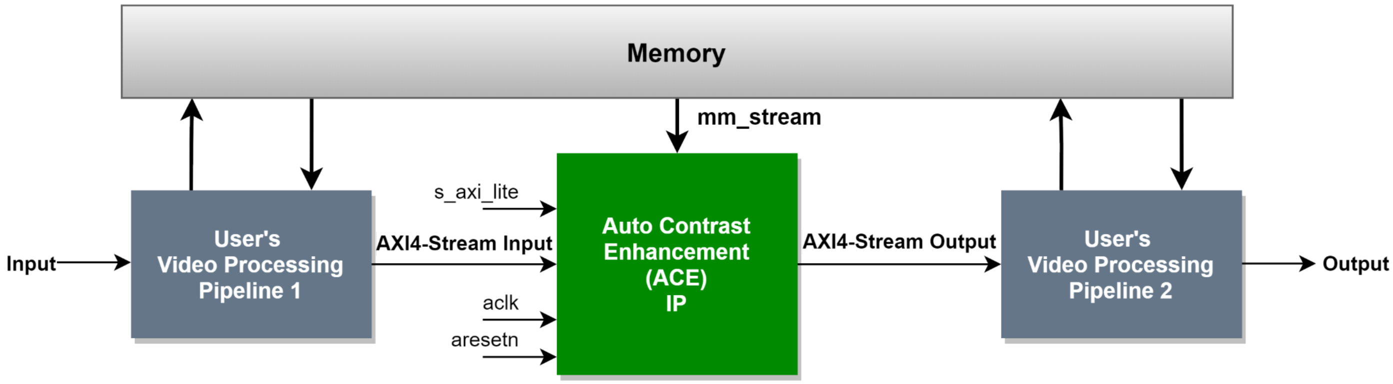


Figure 4. Designing with the ACE IP core

The current version of IP core does not require any IP customization. The core can directly be used in the Vivado IP Integrator.

As the IP has input and output AXI4-Streaming interfaces, the IP can be used before or after or between the user’s video processing pipelines. Memory interfacing is also required for data buffering for histogram analysis of the input stream. The IP needs a single clock to *aclk* pin for both the AXI4-Lite interface and streaming Interface. And the corresponding active low synchronous reset is also required to connect. The IP has an AXI4-Lite interface, which is connected with the master interface of the host processor. This interface is used to configure the IP. Therefore, a software application is required, which initializes, configures and runs the IP with a specific value. The IP does histogram analysis, based on which, the necessity of enhancement of contrast is determined. If it is necessary, then the core performs enhancement otherwise not. This happens automatically without user intervention.

Performance

Maximum Frequencies

The maximum frequencies that the IP core are different due to board types, tool versions and the way of design with the core.

Throughput

The ACE IP core has input and output AXI4-Stream interfaces. The data throttling is bidirectional. The flow of data takes place as long as the source produces valid data and the destination is ready to receive data.

Technically, if *s_axis_tvalid* is not asserted, the ACE core cannot produce valid data. On the other hand, if *m_axis_tready* is not asserted, the core cannot receive valid data from the source. On the contrary, if source is producing valid data, that is, *s_axis_tvalid* is asserted and destination is ready to receive the valid data, that is, *m_axis_tready* is asserted, the ACE IP core generates the valid data, which is indicated by asserting *m_axis_tvalid*. At this moment, the core delivers the 24-bit valid data with one pixel per clock as per *aclk*. The core must be operated at least 148.5MHz clock for the 1080p60 resolution.

Resource Utilization

The FPGA resources consumed by ACE core is summarized as follows;

Board	Xilinx's KC705 Evaluation Board		
Device	xc7k325tffg900-2		
Vivado Version	2019.2		
Resource Utilization			
Site Type	**Available**	**Utilization**	**Utilization %**
Slice	50950	4109	8.06
LUT	203800	11328	5.56
LUTRAM	64000	218	0.34
FF	407600	9107	2.23
DSP	840	40	4.76
BRAM 36K	445	1	0.22
BRAM 18K	890	10	1.12
MMCME2_ADV	10	0	0.00
PLLE2_ADV	10	0	0.00

Table 7. Resource Utilization by ACE IP core

Example Design

This section provides information about the example design with the core. This example design only consists of a synthesizable design.

Synthesizable Design

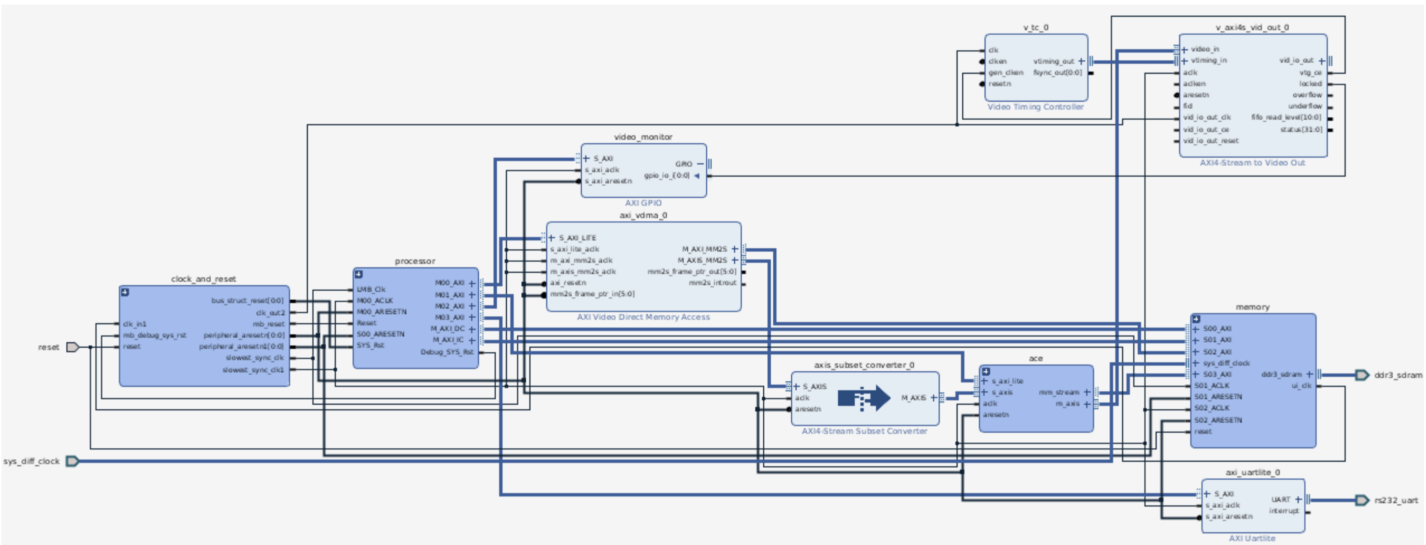


Figure 5. Synthesizable ACE IP core Example Design

The synthesizable example design is shown in the above picture. Please visit the Use Case section to get information about the specific use of the IP core.

Note: This example design is created for the Xilinx KC705 Evaluation board.

In this design, Xilinx Microblaze is used as a host processor. Therefore, a software application is required to run this example. The ACE IP core is interfaced with Microblaze by the AXI4-Lite interface. In this current example design, the low contrast image is stored into the DDR memory, which is read by AXI VDMA core to provide AXI4-Stream input to ACE IP core. Upon receiving the stream, the core does processing and generates the output, which is a contrast-enhanced stream.

The VTC and AXI4-Stream to Video Out are used for outputting the stream in 720p resolution. However, the output is not passed to the real output device; rather, a locked signal from AXI4-stream to Video Out IP is monitored by an AXI GPIO IP to indicate output is obtained successfully or not.

In the SDK part, the layer 1 software APIs are available to initialize and configure the ACE IP core.

Use Case

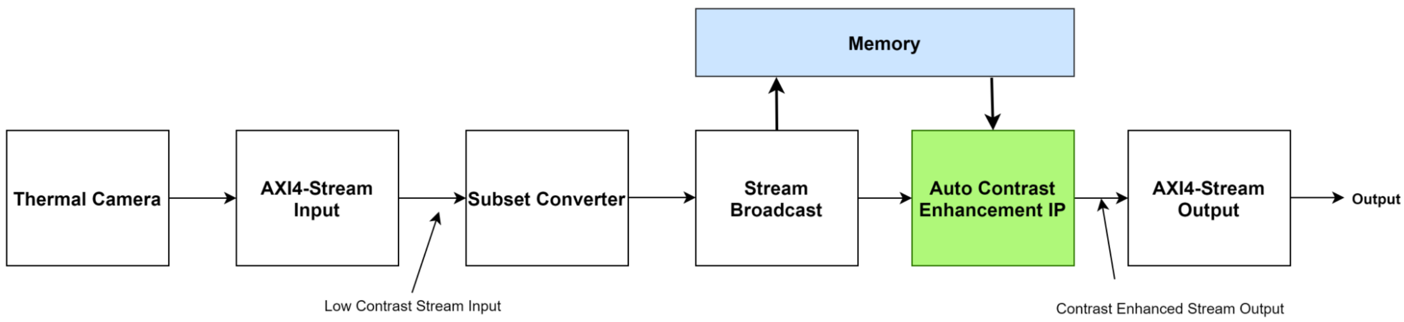


Figure 6. A typical application of ACE IP core

The ACE IP core has applications in many fields such as Machine Vision, Bio-Imaging, Thermal Image etc. The above picture is one of the typical use cases of this IP.

In most cases, the thermal cameras produce low contrast grayscale images, which need contrast enhancement for better image details. For such cases, ACE IP performs very well. The thermal image stream is split into two streams, in which one stream goes memory for buffering and another goes to ACE IP. The buffered image is again accessed by ACE IP to do histogram analysis of input stream while in meantime, the IP parallelly enhances the contrast by utilizing the histogram information. The resulting output is in 24-bit RGB format. The output can be seen on the output device after AXI4-Stream output conversion.

References

1. Vivado Design Suite: AXI Reference Guide (UG1037)
2. AXI Reference Guide (UG761)
3. Vivado Design Suite User Guide: Designing with IP (UG896)
4. Vivado Design Suite User Guide: Getting Started (UG910)
5. Vivado Design Suite User Guide: Programming and Debugging (UG908)
6. Vivado Design Suite User Guide: Implementation (UG904)

Revision History

The following table shows the revision history of this product guide - PGL033.

Date	Version	Detail
August 27, 2021	1.0	Initial Release

Table 8. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution", "Enhancing Financial Trading Algorithms with AI/ML" and "High-Frequency Trading (HFT) based Infrastructure".

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