Introduction

The Non-Uniform Correction IP core is designed to work with a thermal camera to process thermal raw image data and to filter out the fixed pattern noise (FPN) along with adjustment of contrast, brightness and gain. The IP consists of an AXI4-Lite interface which allows easy IP control.

Features

- Configurable parameters such as resolution, contrast, brightness, gain, mode of operation,
- Supports a maximum of 1920x1080 [(1)], resolution with 1 pixel per clock,
- Gain pins for automatic image gain control,
- AXI4-Lite control interface,
- AXI4-MM interface for input,
- Supports 16-bit Monochrome input.
- Supports 16-bits and 14-bit image processing,
- AXI4-Stream interface for output video,
- 16-bit Monochrome video output,

Applications

- Thermal Imaging
- Machine Vision
- CCD, CMOS Thermal camera

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000
Supported User Interfaces	AXI4-Lite, AXI4-Stream, AXI4-MM
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

1. *The example design is provided on 640x480 resolution on email request!*

For IP Support and Interest: sales@logictronix.com or info@logictronix.com

Overview

The Non-Uniform Correction IP is one of the video processing IPs from Logictronix, which is primarily created to process the raw monochrome image data. The IP is especially targeted for thermal cameras such as CCD, CMOS. However, IP can be used on cameras that give raw monochrome image data. The IP supports a maximum of 1920x1080 video resolution.

The IP has AXI4-Lite Interface so that the various parameters like contrast, brightness, gain, mode of operation of IP. The IP also has AXI4-MM interfaces so that IP reads the input image data from the buffer. Upon input image raw data, the IP performs operations such as removal of FPN, adjustment of image gain, brightness, contrast and the final viewable image is obtained from AXI4-Stream interface.

The IP also has gain pins for automatic image gain control. But it depends on the mode of operation of IP.

Port Description

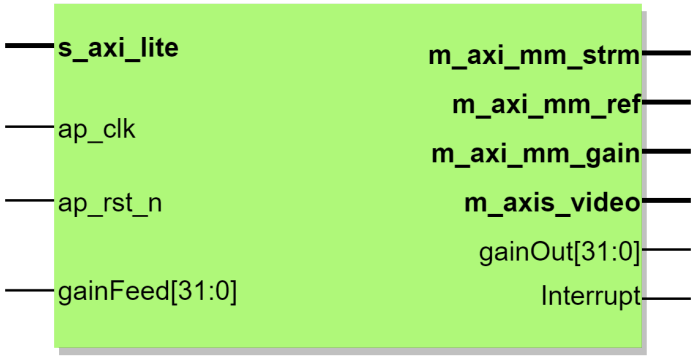


Figure 1. Non-Uniform Correction IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow communication with other IPs or system components. The NUC core ports are described by the following interfaces.

1. Clock, Reset and Interrupt signal Interface

These signals are summarized in the following table.

Signal Name	Width	Direction	Description
ap_clk	1	IN	Core clock
ap_rst_n	1	IN	Core synchronous active low reset
Interrupt	1	OUT	Core Interrupt pin

Table 2. Clock, Reset and Interrupt Signal Interface Description

2. Data Interface

The IP has only one data interface that implements the AXI4-Stream interface protocol. This interface is used to get the data out of the IP. For more information, visit **UG761**.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Signal Name	Width	Direction	Description
m_axis_video_tdata	16	OUT	Output video Data
m_axis_video_tvalid	1	OUT	Output valid
m_axis_video_tready	1	IN	Output ready
m_axis_video_tuser	1	OUT	Output video start of frame
m_axis_video_tlast	1	OUT	Output video end of line
m_axis_video_tstrb	2	OUT	Output video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
m_axis_video_tkeep	2	OUT	Output video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
m_axis_video_tid	1	OUT	Output video data identifier
m_axis_video_tdest	1	OUT	Output video data routing information

Table 3. AXI4-Stream Signal Names and Descriptions

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface. This allows us to configure or control the IP dynamically. This interface will be connected to Zynq PS or Microblaze.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready. INdicates DMA ready to accept the wire address.
s_axi_lite_awaddr	7	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe
s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel. Indicates results of the write transfer
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready. Indicates the target is ready to receive a response.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready. Indicates DMA is ready to accept the read address.
s_axi_lite_araddr	7	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid

s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready. INdicates target is ready to accept the read data.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response. INdicates results of the read transfer.

Table 4. AXI4-Lite Interface Signal Names and Description

4. Memory Interface

The IP consists of three m_axi interfaces for doing the memory read/write operation. These interfaces allow reading the memory data into the IP.
The name and the description of all the memory interfaces are given in the following table.

Signal Name	Width	Direction	Description
m_axi_mm_strm	-	-	Camera raw data. Follow Xilinx’s AXI Reference Guide (UG1037) for more information about AXI4 Signals.
m_axi_mm_ref	-	-	FPN reference image Follow Xilinx’s AXI Reference Guide (UG1037) for more information about AXI4 Signals.
m_axi_mm_gain	-	-	Image gain data Follow Xilinx’s AXI Reference Guide (UG1037) for more information about AXI4 Signals.

Table 5. Memory-mapped AXI4 interface and Description

Register Space

The IP has specific registers so that IP parameters can be set by accessing these registers and then setting the appropriate hex value. The register can be accessed by its offset address. These registers are programmed by AXI4-Lite Interface.

The register name, address and description are given below.

BASEADDR Offset (Hex)	Register Name	Type	Description
0x00	Control Signals	R/W	Bit 0: ap_start Bit 1: ap_done Bit 2: ap_idle Bit 3: ap_ready Bit 7: auto_restart Others: Reserved
0x04	Global Interrupt Enable Register	R/W	Bit 0: Global Interrupt Enable Others: reserved
0x08	IP Interrupt Enable Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x0C	IP Interrupt Status Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x10	m_axis_mm_strm	R/W	32-bit memory address
0x18	m_axis_mm_ref	R/W	32-bit memory address
0x20	m_axis_mm_gain	R/W	32-bit memory address
0x28	active_height	R/W	Number of Active Lines Per Frame
0x30	active_width	R/W	Number of active pixels per scanline
0x38	Brightness	R/W	The brightness of an image frame
0x40	Contrast	R/W	The contrast of an image frame
0x48	Mean	R/W	The mean of an image frame
0x50	Stride	R/W	Pixel Stride value
0x58	Mode	R/W	Mode of operation of IP
0x60	Divisor	R/W	Contrast Divisor to set the contrast precisely with

			decimal precision

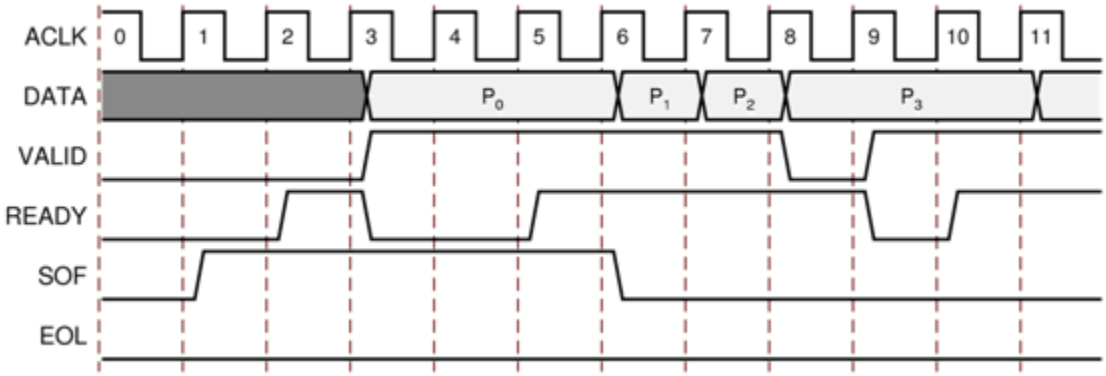
Table 6. IP Register Names, Offset Addresses and Descriptions

Video Data

The IP generates monochrome video data with 1 pixel per clock and 16-bits per component through the *m_axis_video* port. A subset converter IP can be used to get video data in the required RGB format

Figure 2. Single Pixel Per Clock, 16-bits per component Monochrome Video Data Format

Data Flow



**Ref. Xilinx's PG103*

Figure 3. AXI4-Stream Data flow mechanism

The flow of data mainly occurs by the four signals. They are; *m_axis_video_tvalid*, *m_axis_video_tready*, *m_axi_video_tuser* (SOF) and *m_axi_video_tlast* (EOL). These signals are called AXI4-stream handshaking signals.

For a complete transfer of the image frame, the SOF signal must be high, which indicates the beginning of the frame. During this moment, *m_axis_video_tready* and *m_axi_video_tvalid* must be at HIGH state to begin the flow of valid data from this IP (master) to receiving IP (slave). EOL is asserted HIGH when the transfer of pixels per scanline is completed.

Designing with the NUC IP Core

The design with the core has been summarized in the following picture.

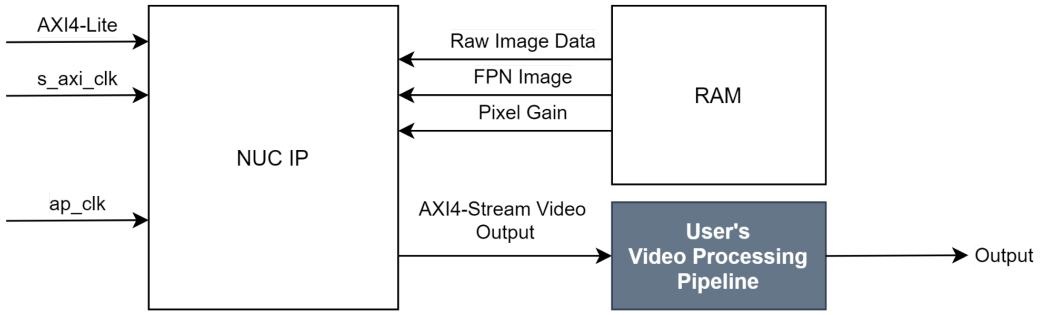


Figure 4. Designing with the NUC IP core

The core does not require any customization. The core can directly be used in the Vivado IP Integrator.

The IP needs two clocks for the AXI4-Lite interface and streaming Interface. And the corresponding synchronous resets are also required to connect. The IP has an AXI4-Lite interface, which is connected with the master interface of the host processor. This interface is used to configure the IP. This means, a software application is required, which initializes, configures and runs the IP with a specific value. Similarly, three memory-mapped AXI4 master interfaces of IP are used to read data from the memory. This data includes image related information such as raw image data, reference image and pixel gain.

The IP does the processing of raw image data, where FPN is removed, image contrast, brightness and gain are adjusted and then generates a viewable image. The image adjustment is needed to do by the user by giving the appropriate values. The final video data is streamed out by the AXI4-Stream video output interface of the IP. This output can be fed to user-specific video processing IPs or the pipe to do specific video processing.

The IP mode of operation can be set by giving a value from 1 to 4. Modes 1 and 2 are to operate IP for 16-bit or 14-bit images with gain control disabled respectively. And similarly, modes 3 and 4 are to operate IP for 16-bit or 14-bit images with gain control enabled respectively. In automatic mode, gain pins are used for gain feedback.

Performance

Maximum Frequencies

The maximum frequencies that the IP core can be operated on are found to be different due to board types, tool versions and the way of design with the core.

Throughput

The NUC IP core has an output AXI4-Stream interface only acting as a source of data. The flow of data takes place with AXI4-stream handshaking signals. The IP core generates the valid data as per processing, which is indicated by *m_axis_video_tvalid* at a HIGH state. However, until the slave interface is ready, the data is not transmitted. The slave state is indicated by the *m_axi_video_tready* line. According to AXI4-Protocol, the valid data transfer occurs when both signals are at HIGH states. At this stage, the core delivers the 16-bit data with one pixel per clock as per *ap_clk*.

Resource Utilization

The FPGA resources consumed by the NUC core is summarized as follows;

Board	Xilinx's KC705 Evaluation Board		
Device	xc7k325tffg900-2		
Vivado Version	2019.2		
Resource Utilization			
Site Type	**Available**	**Utilization**	**Utilization %**
Slice	50950	3754	8.26
LUT	203800	10767	5.28
LUTRAM	64000	309	0.48
FF	407600	8665	2.13
DSP	840	17	2.02
BRAM 36K	445	15	3.37
BRAM 18K	890	0	0.00
MMCME2_ADV	10	0	0.00
PLLE2_ADV	10	0	0.00

Table 7. Resource Utilization by NUC core

Example Design

This section provides the example design with the core. This example design only consists of a synthesizable design.

Synthesizable Design

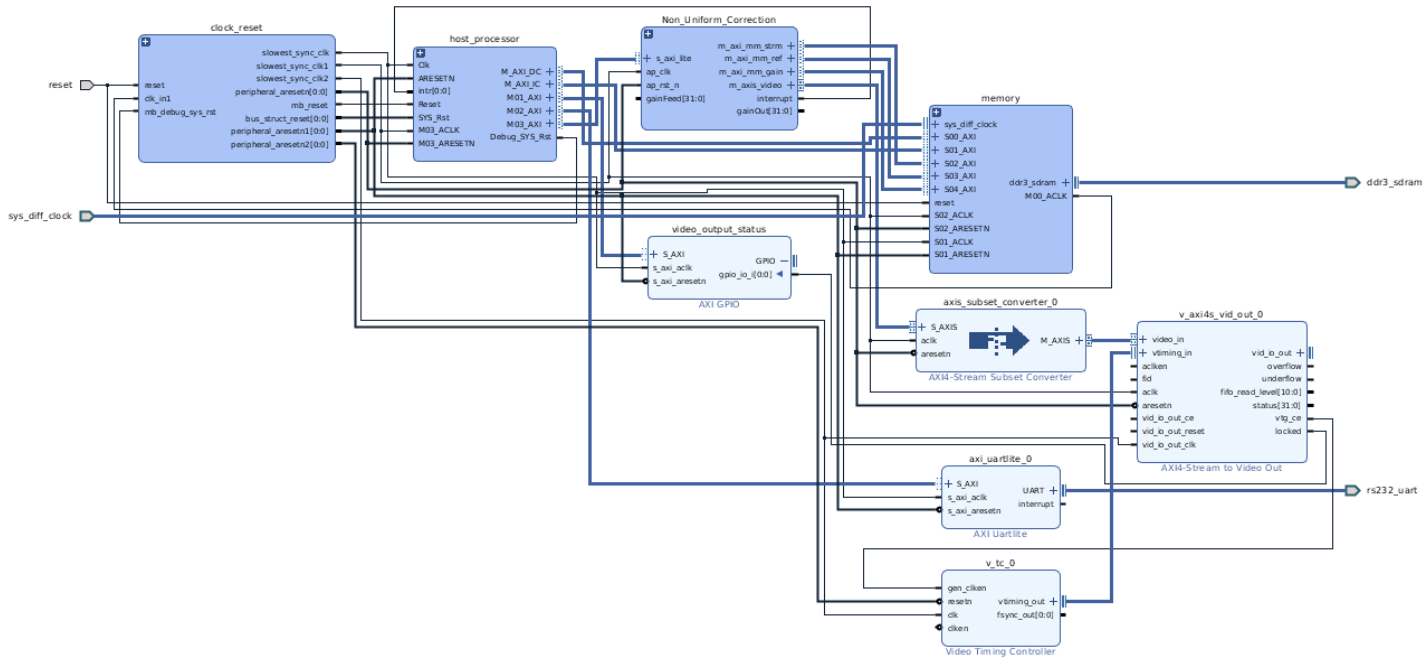


Figure 5. Synthesizable NUC IP core Example Design

The synthesizable example design is shown in the above picture.

Note: This example design is created for the Xilinx KC705 Evaluation board.

In this design, Xilinx Microblaze is used as a host processor. Therefore, a software application is required to run this example. The NUC IP core is interfaced with Microblaze and memory by AXI4-Lite interface and Memory-mapped AXI4 port respectively. The image input data is loaded into the DDR memory so that the NUC core gets those data and processes them to get output in AXI4-Stream format. An AXI4-Stream Subset Converter IP is used to get streams in RGB format as the NUC core gives monochrome data. The VTC and AXI4-Stream to Video Out are used for getting video output. The IP core supports a maximum of 1920x1080 resolution. However, the design is tested with a 480p resolution. The output is not passed to the real output device; rather, a locked signal from AXI4-stream to Video Out IP is monitored by an AXI GPIO IP to indicate output is obtained successfully or not.

In the SDK part, the NUC core has to be initialized and the initial parameters such as contrast, brightness and reference image mean, mode and contrast divisor value have to be initialized. These are just initial parameters because these values eventually have to be adjusted by the user for fine-tuning the final output.

Use Case

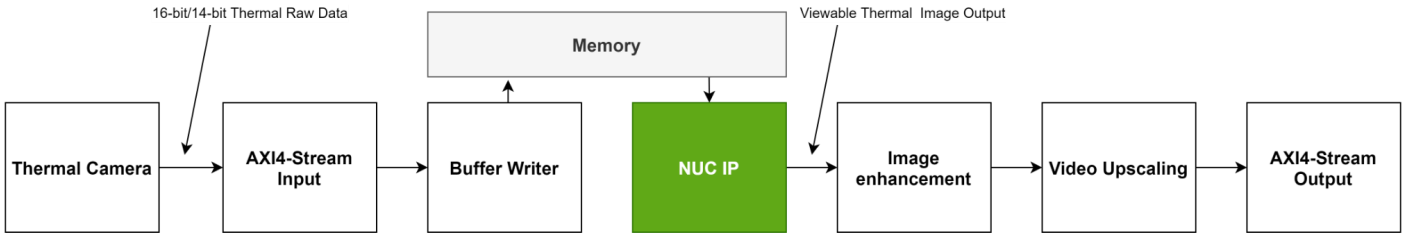


Figure 6. Typical Use Case of design with NUC core

A typical use case of NUC IP is shown above. A thermal camera data is taken. This data includes pixel clock, HS, VS, Active_Data. The data is actually the 16-bit/14-bit raw thermal data, which is needed to process. The data is converted into AXI4-Stream format, which is written into the specific location in the buffer by buffer writer block.

On the other hand, the NUC IP has memory-mapped AXI4 interfaces, which can be configured to read back those memory data into the IP and process them to get a viewable thermal image in the AXI4-Stream format. The output can further be enhanced by applying image enhancement techniques. And video upscaling is done in order to scale up the video resolution from 480p to desired resolution. Finally, the output can be obtained after AXI4-Stream to Video output conversion.

References

1. Vivado Design Suite: AXI Reference Guide (UG1037)
2. AXI Reference Guide (UG761)
3. Vivado Design Suite User Guide: Designing with IP (UG896)
4. Vivado Design Suite User Guide: Getting Started (UG910)
5. Vivado Design Suite User Guide: Programming and Debugging (UG908)
6. Vivado Design Suite User Guide: Implementation (UG904)

Revision History

The following table shows the revision history of this product guide - PGL031.

Date	Version	Detail
August 13, 2021	1.0	Initial Release

Table 8. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including ANPR Solution", "Enhancing Financial Trading Algorithms with AI/ML" and "High-Frequency Trading (HFT) based Infrastructure".

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