

Introduction

The IP core is designed to recreate an RGB color image from a Bayer image. This IP can be used to interface with different digital camera sensors that produce Bayer pattern image output.

Features

- Generates RGB color output.
- Configurable parameters such as resolution, color output selection,
- Supports a maximum of 1920x1080, resolution with 1 pixel per clock,
- AXI4-Lite control interface,
- AXI4-Stream interface for input and output video,
- Supports 24-bit input and output streams.

Applications

- Digital Image Camera
- Machine Vision

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

Overview

Most digital cameras use Bayer Filter to produce final color images. Initially, the image is in the form of a Bayer pattern, which has a single color component for a pixel. Later on in the processing, the missing color components are determined for every pixel of an image. And the result will be an RGB color image. This is what Bayer to RGB IP does. The IP determines all the missing color components and produces an RGB color image. This is also called Demosaicking.

The IP supports a maximum of 1920x1080 video resolution. This value can be set by the AXI4-Lite interface. The IP has AXI4-compliant input and output stream interfaces. These interfaces support a 24-bit RGB format. The IP currently supports BGGR Bayer pattern images. However, other Bayer pattern support features along with other IP features will be included as per the customer requirement.

Port Description



Figure 1. Bayer to RGB IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow communication with other IPs or system components. The TCP core ports are described by the following interfaces.

1. Clock, Reset and Interrupt signal Interface

These signals are summarized in the following table.

Signal Name	Width	Direction	Description
ap_clk	1	IN	Core clock for both AXI4-Stream as well as AXI4-Lite Interface
ap_rst_n	1	IN	Core ap_clk synchronous active low reset
Interrupt	1	OUT	Core Interrupt pin

Table 2. Clock, Reset and Interrupt Signal Interface Description

2. Video Interface

The IP has two data interfaces *s_axis* and *m_axis* that implement the AXI4-Stream interface protocol. These interfaces are used to get input as well as output stream data respectively.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Signal Name	Width	Direction	Description
AXI4-Stream Input Signals			
<i>s_axis_tdata</i>	24	OUT	Input video Data
<i>s_axis_tvalid</i>	1	OUT	Input valid
<i>s_axis_tready</i>	1	IN	Input ready
<i>s_axis_tuser</i>	1	OUT	Input video start of frame
<i>s_axis_tlast</i>	1	OUT	Input video end of line
<i>s_axis_tstrb</i>	3	OUT	Input video data strobe indicates whether the content of the associated byte of <i>tdata</i> is processed as a data byte or position byte
<i>s_axis_tkeep</i>	3	OUT	Input video byte qualifier that indicates whether the content of the associated byte of <i>tdata</i> is processed as part of the data stream
<i>ss_axis_tid</i>	1	OUT	Input video data identifier
<i>s_axis_tdest</i>	1	OUT	Input video data routing information
AXI4-Stream Output Signals			
<i>m_axis_tdata</i>	24	OUT	Output video Data
<i>m_axis_tvalid</i>	1	OUT	Output valid
<i>m_axis_tready</i>	1	IN	Output ready
<i>m_axis_tuser</i>	1	OUT	Output video start of frame
<i>m_axis_tlast</i>	1	OUT	Output video end of line

m_axis_tstrb	3	OUT	Output video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
m_axis_keep	3	OUT	Output video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
m_axis_tid	1	OUT	Output video data identifier
m_axis_tdest	1	OUT	Output video data routing information

Table 3. AXI4-Stream Signal Names and Descriptions

Both streaming interfaces run at *ap_clk*.

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface. This allows us to configure or control the IP dynamically. This interface will be connected to Zynq PS or Microblaze.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready. INDicates DMA ready to accept the wire address.
s_axi_lite_awaddr	6	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe

s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel. Indicates results of the write transfer
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready. This indicates the target is ready to receive a response.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready. Indicates DMA is ready to accept the read address.
s_axi_lite_araddr	6	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.

Table 4. AXI4-Lite Interface Signal Names and Description

This interface also runs at the ap_clk clock.

Register Space

The IP has specific registers so that IP parameters can be set by accessing these registers and then setting the appropriate hex value. The register can be accessed by its offset address. These registers are programmed by AXI4-Lite Interface. When IP APIs are not available, the IP can be operated by using the register.

The register name, address and description are given below.

BASEADDR Offset (Hex)	Register Name	Type	Description
0x00	Control Signals	R/W	Bit 0: ap_start Bit 1: ap_done Bit 2: ap_idle Bit 3: ap_ready Bit 7: auto_restart Others: Reserved
0x04	Global Interrupt Enable Register	R/W	Bit 0: Global Interrupt Enable Others: reserved
0x08	IP Interrupt Enable Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x0C	IP Interrupt Status Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready) Others: Reserved
0x10	active_height	R/W	Number of Active Lines Per Frame
0x18	active_width	R/W	Number of active pixels per scanline
0x20	mode	R/W	To set output mode

Table 5. IP Register Names, Offset Addresses and Descriptions

Video Data

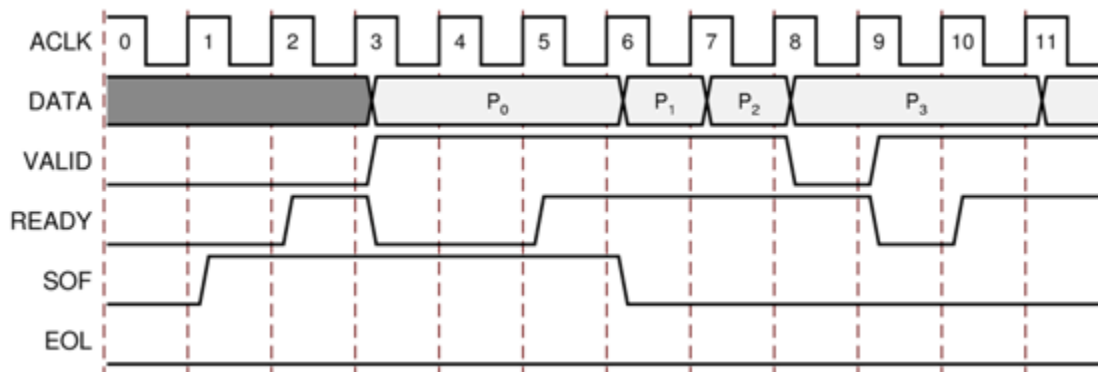
The core generates RGB video data with 1 pixel per clock and 8-bits per component through the *m_axis* port.



Figure 2. Single Pixel Per Clock, 8-bits per component RGB Video Data Format

Note: Currently IP generates pixel data with 8-bit per color component. However, the IP will be updated to support 10-bit, 12-bit and 16-bit in the future version of IP.

Data Flow



*Ref. Xilinx's PG103

Figure 3. AXI4-Stream Data flow mechanism

The flow of data is according to AXI4-Stream protocol, which mainly occurs by the four signals in the current IP design. They are; *m_axis_tvalid*, *m_axis_tready*, *m_axis_tuser* (SOF) and *m_axis_tlast* (EOL). These signals are called AXI4-stream handshaking signals. The data is carried out by *m_axis_tdata*.

For a complete transfer of the frame, the SOF signal goes high, which indicates the beginning of the frame. During this moment, *m_axis_tready* and *m_axis_tvalid* must be at HIGH state to begin the flow of valid data from this IP (master) to receiving IP (slave). EOL is asserted HIGH when the transfer of pixels per scanline is completed.

Designing with the Byr2RGB IP core

The design with the core has been summarized in the following picture.

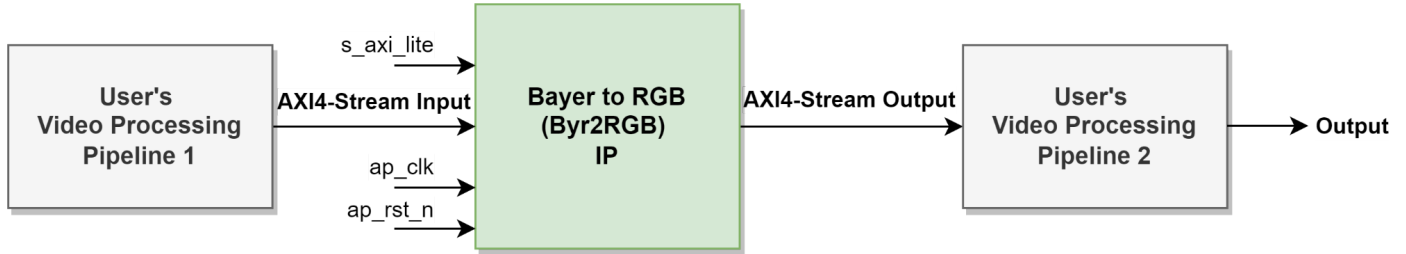


Figure 4. Designing with the Byr2RGB IP core

The IP gets input from the user's video processing pipeline 1, which can be a digital camera sensor interface or memory-mapped interface or any other Bayer pattern image source.

The IP needs a single clock for both the AXI4-Lite interface and streaming Interface. And the corresponding active low synchronous reset is also required to connect. The IP has an AXI4-Lite interface, which is connected with the master interface of the host processor. This interface is used to configure the IP. Therefore, a software application is required, which initializes, configures and runs the IP with a specific parameter. There are two output modes available. Mode 0 is to output Bayer image without processing. Mode 1 is to output an RGB image.

Performance

Maximum Frequencies

The maximum frequencies that the IP core can be operated on are different due to board types, tool versions and the way of design with the core.

Throughput

The Byr2RGB IP core has input and output AXI4-Stream interfaces. The data throttling is bidirectional between input and output interfaces. In other words, the flow of data takes place as long as the source produces valid data and the destination is ready to receive data.

Technically, if *s_axis_tvalid* is not asserted, the Byr2RGB core cannot produce valid data. On the other hand, if *m_axis_tready* is not asserted, the core cannot receive valid data from the source. On the contrary, if the source is producing valid data, that is, *s_axis_tvalid* is asserted and destination is ready to receive the valid data, that is, *m_axis_tready* is asserted, the Byr2RGB IP core generates the valid data, which is indicated by asserting *m_axis_tvalid*. At this moment, the core delivers the 24-bit valid data with one pixel per clock as per *ap_clk*. The core must be operated at least 148.5MHz clock for the 1080p60 resolution.

Resource Utilization

The FPGA resources consumed by Byr2RGB core is summarized as follows;

Board	Xilinx's KC705 Evaluation Board		
Device	xc7k325tffg900-2		
Vivado Version	2019.2		
Resource Utilization			
Site Type	Available	Utilization	Utilization %
Slice	50950	263	0.52
LUT	203800	586	0.29
LUTRAM	64000	0	0.00
FF	407600	826	0.20
DSP	840	2	0.24
BRAM 36K	445	1	0.22
BRAM 18K	890	2	0.22

MMCME2_ADV	10	0	0.00
PLLE2_ADV	10	0	0.00

Table 6. Resource Utilization by Byr2RGB core

Use Case

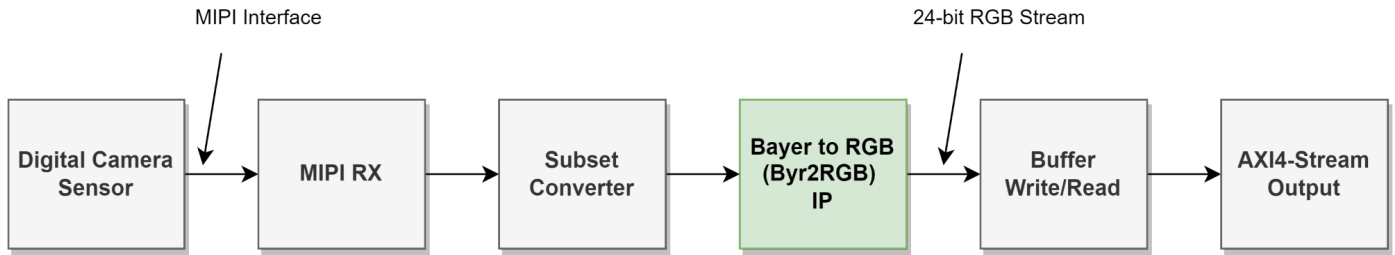


Figure 6. Typical application of Bry2RGB IP core

The above picture is one of the use cases of this IP. The IP is designed to convert the Bayer image to the RGB color output. MIPI digital camera sensor generates specific Bayer pattern image. This can be fed into the system by MIPI IP. The image data is in the monochrome format, which is converted to grayscale format by subset conversion. Finally, the stream is sent to Byr2RGB IP, which in turn generates 24-bit RGB color output.

References

1. Vivado Design Suite: AXI Reference Guide ([UG1037](#))
2. AXI Reference Guide ([UG761](#))
3. Vivado Design Suite User Guide: Designing with IP ([UG896](#))
4. Vivado Design Suite User Guide: Getting Started ([UG910](#))
5. Vivado Design Suite User Guide: Programming and Debugging ([UG908](#))
6. Vivado Design Suite User Guide: Implementation ([UG904](#))

Revision History

The following table shows the revision history of this product guide - PGL034.

Date	Version	Detail
Dec 6, 2021	1.0	Initial Release

Table 7. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution", "Enhancing Financial Trading Algorithms with AI/ML" and "High-Frequency Trading (HFT) based Infrastructure".

For IP Licensing, Sales and Support: **Contact**

LogicTronix Technologies Pvt. Ltd.

Koupondole-10, Lalitpur, Nepal

Email: sales@logictronix.com

Web: www.LogicTronix.com