

Introduction

The IP core takes AXI4-Stream as input and produces the gamma corrected stream output particularly based on gamma correction value.

Features

- Most LCD monitors have gamma value of 2.2 and for most of the standard monitor gamma value for Mac OS is 1.8,
- Nowadays, the gamma value of 2.2 is standard for all Windows and MacOS monitors,
- Corrects the gamma according to the gamma level,
- Configurable parameters such as resolution, gamma value,
- Supports a maximum of 1920x1080, resolution with 1 pixel per clock,
- AXI4-Lite control interface,
- AXI4-Stream interface for input and output video,
- Supports 24-bit RGB input and output.

Applications

- Thermal Imaging
- Machine Vision
- Digital Camera Sensor
- CCD, CMOS Thermal camera
- Industrial Thermal Inspection

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000, *UltraScale/UltraScale+
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

** For >1080p resolution support, please contact us !*

Overview

The Gamma Correction (GMC) IP core is created for correcting the gamma level of the input image according to the gamma value provided. This IP can be used on any AXI4-Stream source that gives RGB video/image output. The IP supports a maximum of 1920x1080 video resolution. The IP has AXI4-compliant input and output stream interfaces. These interfaces support a 24-bit RGB format.

The IP has an AXI4-Lite Interface which provides better control over the IP. This interface allows setting the video resolution and gamma level.

Port Description



Figure 1. Gamma Correction IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow communication with other IPs or system components. The core ports are described by the following interfaces.

1. Clock, Reset and Interrupt signal Interface

These signals are summarized in the following table.

Signal Name	Width	Direction	Description
ap_clk	1	IN	Core clock for both AXI4-Stream as well as AXI4-Lite Interface
ap_rst_n	1	IN	Core ap_clk synchronous active low reset
Interrupt	1	OUT	Core Interrupt pin

Table 2. Clock, Reset and Interrupt Signal Interface Description

2. Video Interface

The IP has *s_axis* and *m_axis* interfaces that implement the AXI4-Stream interface protocol. These interfaces are used to get input as well as output stream data respectively.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Signal Name	Width	Direction	Description
AXI4-Stream Input Signals			
<i>s_axis_tdata</i>	24	IN	Input video Data
<i>s_axis_tvalid</i>	1	IN	Input valid
<i>s_axis_tready</i>	1	OUT	Input ready
<i>s_axis_tuser</i>	1	IN	Input video start of frame
<i>s_axis_tlast</i>	1	IN	Input video end of line
<i>s_axis_tstrb</i>	3	IN	Input video data strobe indicates whether the content of the associated byte of <i>tdata</i> is processed as a data byte or position byte
<i>s_axis_tkeep</i>	3	IN	Input video byte qualifier that indicates whether the content of the associated byte of <i>tdata</i> is processed as part of the data stream
<i>s_axis_tid</i>	1	IN	Input video data identifier
<i>s_axis_tdest</i>	1	IN	Input video data routing information
AXI4-Stream Output Signals			
<i>m_axis_tdata</i>	24	OUT	Output video Data
<i>m_axis_tvalid</i>	1	OUT	Output valid
<i>m_axis_tready</i>	1	IN	Output ready
<i>m_axis_tuser</i>	1	OUT	Output video start of frame
<i>m_axis_tlast</i>	1	OUT	Output video end of line

m_axis_tstrb	3	OUT	Output video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
m_axis_keep	3	OUT	Output video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
m_axis_tid	1	OUT	Output video data identifier
m_axis_tdest	1	OUT	Output video data routing information

Table 3. AXI4-Stream Signal Names and Descriptions

All streaming interfaces run at *ap_clk*.

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready. INDicates DMA ready to accept the wire address.
s_axi_lite_awaddr	6	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe

s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel. Indicates results of the write transfer
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready. This indicates the target is ready to receive a response.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready. Indicates DMA is ready to accept the read address.
s_axi_lite_araddr	6	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.

Table 4. AXI4-Lite Interface Signal Names and Description

This interface also runs at the ap_clk clock.

Register Space

The IP has been generated with built-in registers. These registers must be programmed so that IP can do its job. At the IP hardware level, these registers are accessed by their addresses. These registers are programmed by AXI4-Lite Interface. When IP software APIs are not available, the IP can be operated by using the register.

The register name, address and description are given below.

BASEADDR Offset (Hex)	Register Name	Type	Description
0x00	Control Signals	R/W	Bit 0: ap_start Bit 1: ap_done Bit 2: ap_idle Bit 3: ap_ready Bit 7: auto_restart
0x04	Global Interrupt Enable Register	R/W	Bit 0: Global Interrupt Enable
0x08	IP Interrupt Enable Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready)
0x0C	IP Interrupt Status Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready)
0x10	Gamma	R/W	Gamma value of the input stream
0x18	Height	R/W	Number of Active Lines Per Frame
0x20	Width	R/W	Number of active pixels per scanline

Table 5. IP Register Names, Offset Addresses and Descriptions

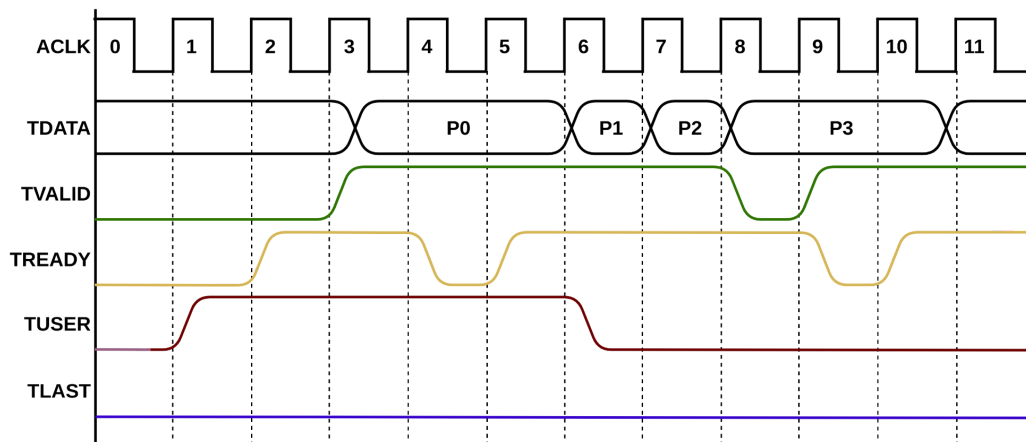
Video Data

The core generates RGB video data with 1 pixel per clock and 8-bits per component through the *m_axis* port.



Figure 2. Single Pixel Per Clock, 8-bits per component RGB Video Data Format

Data Flow



*Ref. Xilinx's PG103

Figure 3. AXI4-Stream Data flow mechanism

The flow of data is according to AXI4-Stream protocol, which mainly occurs by *m_axis_tvalid*, *m_axis_tready*, *m_axis_tuser* (SOF) and *m_axis_tlast* (EOL) signals. Stream flow occurs by handshaking. The data is carried out by *m_axis_tdata*.

For a complete transfer of the frame, the SOF signal goes high, which indicates the beginning of the frame. During this moment, *m_axis_tready* and *m_axis_tvalid* must be at HIGH state to begin the flow of valid data from this IP (master) to receiving IP (slave). EOL is asserted HIGH when the transfer of pixels per scanline is completed.

Designing with the Gamma Correction IP core

The design with the core has been summarized by the following picture.

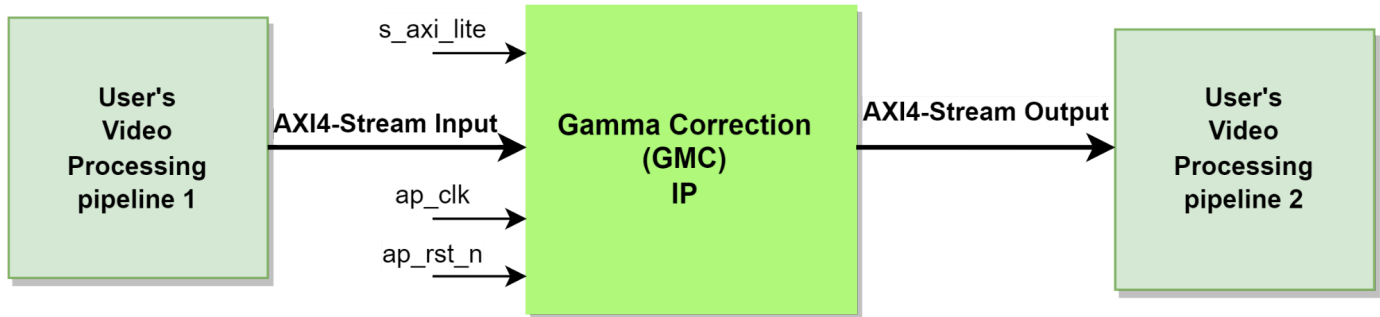


Figure 4. Designing with the Gamma Correction IP core

The IP needs a single clock for both the AXI4-Lite interface and streaming Interface. And the corresponding active low synchronous reset is also required to connect. The IP is configured through the AXI4-Lite interface. Therefore, a software application is required. User has to set the stream resolution and the gamma value from 0 to 9 which then selects the gamma level.

Performance

Maximum Frequencies

The maximum frequencies that the IP core can be operated on are different due to board types, tool versions and the way of design with the core.

Throughput

Since the GMC IP core has input and output AXI4-Stream interfaces, the data throttling is bidirectional. When the source produces valid data and the destination is ready to receive data, the actual data flow takes place. This flow of data is AXI4-complaint based.

If *s_axis_tvalid* is not asserted, the GMC core cannot produce valid data for slave IP (destination) and if *m_axis_tready* is not asserted, the core cannot receive valid data from the master IP (source). In this way, if source is producing valid data, indicated by *s_axis_tvalid* HIGH and destination is ready to receive the valid data, indicated by *m_axis_tready* HIGH, the GMC IP core generates the valid data, indicated by asserting *m_axis_tvalid*. At this moment, the core delivers the 24-bit valid data with one pixel per clock as per *ap_clk*. The core must be operated at least 148.5MHz clock for the 1080p60 resolution.

Resource Utilization

The FPGA resources consumed by Gamma Correction IP core is summarized as follows;

Board	Xilinx's ZC706 Evaluation Board		
Device	xc7z045ffg900-2		
Vivado Version	2019.1		
Resource Utilization			
Site Type	Available	Utilization	Utilization %
Slice	54650	0	0.00
LUT	218600	344	0.16
LUTRAM	70400	0	0.00
FF	437200	483	0.11
DSP	900	0	0.00

BRAM 36K	545	0	0.00
BRAM 18K	1090	18	1.65
MMCME2_ADV	8	0	0.00
PLLE2_ADV	8	0	0.00

Table 6. Resource Utilization by Gamma Correction core

Example Design

This section provides information about the example design with the core. This example design only consists of a synthesizable design.

Synthesizable Design

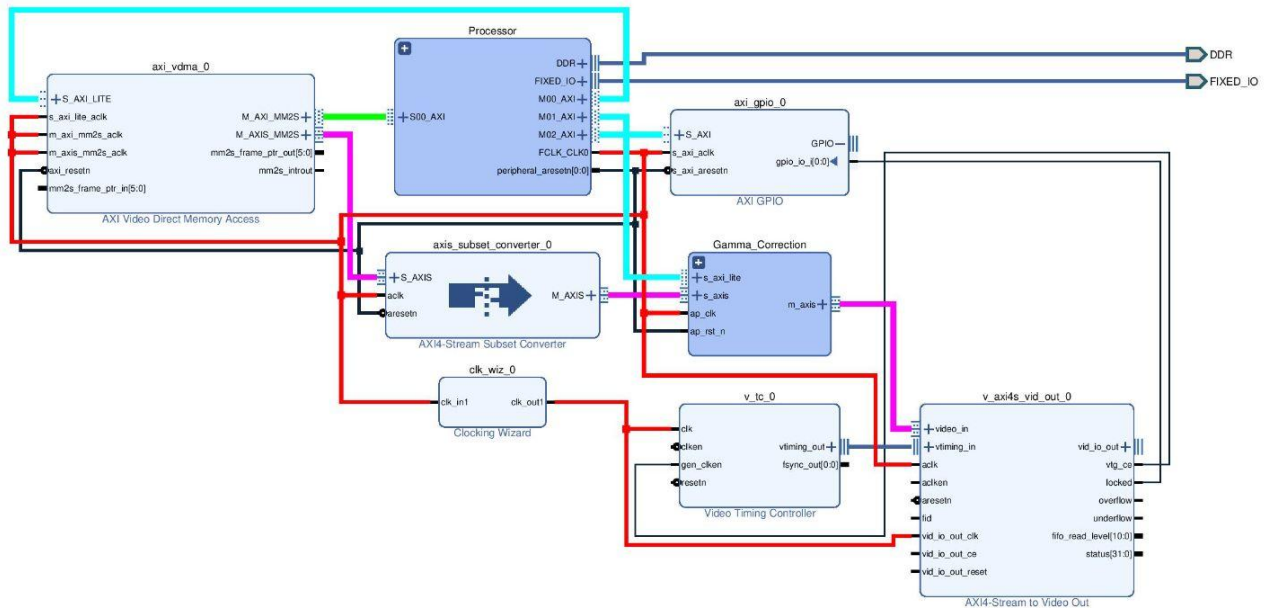


Figure 5. Synthesizable Gamma Correction IP core Example Design

The synthesizable example design is shown in the above picture. You can visit the Use Case section to get information about the specific use of the IP core.

Note: This example design is created for the **Xilinx ZC706 Evaluation board**.

This design represents the AXI4-Memory-Mapped based example design. The memory-mapped data of the input image must be loaded into the DDR memory. Memory-mapped-to-Stream (MM2S) conversion is required so that stream data can be given to GMC IP. For this requirement, VDMA is used with a read channel enabled with 32-bit data width customization. Upon receiving AXI4-Stream as input and gamma value setup, the GMC IP core generates a 24-bit gamma corrected output stream.

The VTC and AXI4-Stream to Video Out are used for outputting the stream in 1080p resolution. A locked signal from AXI4-stream to Video Out IP is monitored by an AXI GPIO IP to indicate output is obtained successfully or not.

In the SDK part, the layer 1 software APIs are available to initialize and configure the Gamma Correction IP core. The API enables or disables interrupt, set stream resolution and gamma value.

Use Case

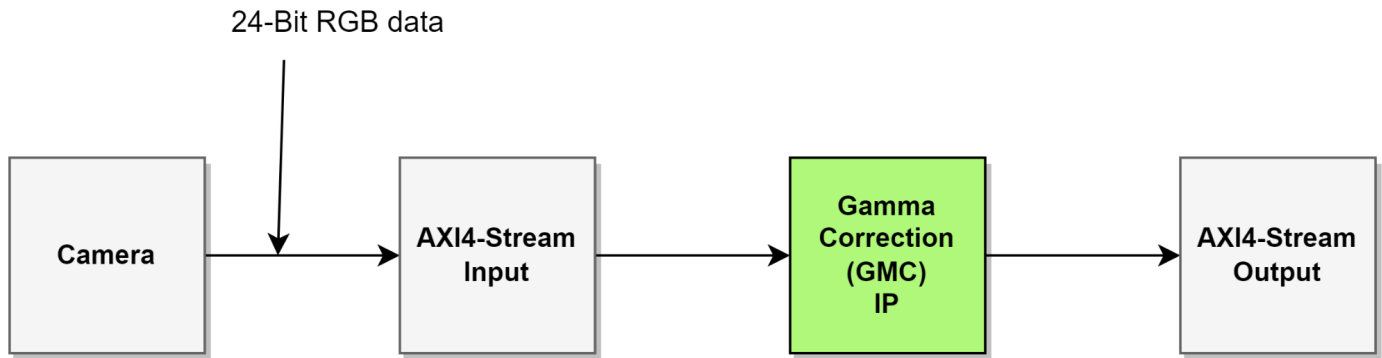


Figure 6. Typical application of Gamma Correction IP core

The above picture shows a general use-case of the GMC IP core. In real-life, the gamma correction comes under post-image enhancement technique. In most camera sensor interfacing, the sensor does not itself produce well-tuned output images. For such a scenario, several post-image processing algorithms might be required to tune the image perfectly. When global brightness is required, then a gamma correction algorithm comes into the major role and this is what is achieved by GMC IP. This IP core becomes a wise choice for FPGA based image processing.

To use and apply gamma correction, GMC IP core requires AXI4-complaint input image, which means that the camera data needed to be in AXI4-Stream. And oppositely, to get gamma corrected image displayed, the AXI4-Stream is needed to convert into 24-bit Native Video format.

References

1. Vivado Design Suite: AXI Reference Guide ([UG1037](#))
2. AXI Reference Guide ([UG761](#))
3. Vivado Design Suite User Guide: Designing with IP ([UG896](#))
4. Vivado Design Suite User Guide: Getting Started ([UG910](#))
5. Vivado Design Suite User Guide: Programming and Debugging ([UG908](#))
6. Vivado Design Suite User Guide: Implementation ([UG904](#))

Revision History

The following table shows the revision history of this product guide - PGL037.

Date	Version	Detail
December 28, 2021	1.0	Initial Release

Table 7. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution", "Enhancing Financial Trading Algorithms with AI/ML" and "High-Frequency Trading (HFT) based Infrastructure".

For IP Licensing, Sales and Support: **Contact**

LogicTronix Technologies Pvt. Ltd.

Xilinx Certified Partner

Email: ip-sales@logictronix.com

Web: www.LogicTronix.com