

Training on "Machine Learning Acceleration with Xilinx Vitis/Petalinux and MPSoC FPGA [Ultra96V2 FPGA]"

Training Hours: 60 Credit Hour

Training Outlines Document- LogicTronix [Released- external]

January 2022

Training Outlines-Main Session [30 Credit Hour]

1. Introduction to VIVADO IP design flow.
2. Introduction to HLS IP design method and integrating HLS IP to VIVADO IPI flow.
3. Exporting VIVADO XSA and crating Software application [s/w application is optional].
4. Developing Petalinux build for the XSA.
5. Integrating Petalinux and VIVADP XSA or XCLBIN into Vitis Tool and writing application for it.
6. Understanding the Vitis AI flow and ML models provided by Xilinx at Model Zoo.
7. Building application and testing on Ultra96v2 using UART or SSH or MiniDPDisplay.
8. Creating own NN architecture or model, training it on GPU or CPU, creating freeze model in GPU or CPU, writing inferencing script and running it on GPU or CPU architecture. Running inferencing on GPU or CPU.
9. Understanding of Vitis AI Quantizer and Optimizer. Now quantizing or converting the freeze model.
10. Basic understanding of custom pruning method and quantization method for Darknet or Tensorflow framework based NN architecture.
11. Now writing Vitis application for this NN model based on "point 3 based VIVADO design" and "point 4 based Petalinux".
12. Testing of ML application on MPSoC FPGA Board.

Advanced Training Sessions- Outlines [30 Credit Hour]

1. Integrating custom HLS IP, creating VIVADO design.
2. Petalinux design with device tree and custom application.
3. Creating Vitis ML application with multi-threading and multi-processing.
4. Using GStreamer for GUI development for "edge detection" and custom ML application,
5. Using VCU based design for encoding and decoding, example design development and testing with ZU4EV or higher FPGA boards.
6. GUI development with real time camera stream processing with VCU and implementing Machine Learning on detection, classification and recognition type of application.

Revision History

The following table shows the revision history of this **Training Outline – TOL011**.

Date	Version	Detail
January 6, 2022	2.0	Revised outlines for more MPSoC Boards
July 18, 2021	1.2	Initial Release (Public)
August 20, 2020	1.1	Internal Release (Migrated from DNNDK into Vitis Flow)

Table 8. Training Outline Revision History

About LogicTronix

LogicTronix provides turnkey Solutions, design services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Learning Acceleration for various applications including ADAS, Surveillance, Computer Vision, etc.

LogicTronix also offers solutions on “Real-Time Traffic Video Analytics Solution (TVAS) - including ANPR Solution”, “Enhancing Financial Trading Algorithms with AI/ML” and “High Frequency Trading (HFT) based Infrastructure”.

For Trainings, IP Licensing, Sales and Support: **Contact**

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FPGA Design and Machine Learning Company

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