Introduction

The IP core takes images from the AXI4-Stream source and then enhances global sharpness. The IP consists of AXI4-Lite and AXI4-Stream interfaces which allow easy IP integration in Vivado BD.

Features

- Enhances the sharpness of the image.
- Configurable parameters such as resolution,
- Supports a maximum of 1920x1080, resolution with 1 pixel per clock,
- AXI4-Lite control interface,
- AXI4-Stream interface for input and output video,
- Supports 24-bit RGB input and output.

Applications

- Thermal Imaging
- Machine Vision
- Medical Imaging
- Digital Camera Sensor

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000, *UltraScale/UltraScale+
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

** For >1080p resolution support, please contact us !*

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Overview

The Sharp Enhancement (SEN) IP is one of the video processing IPs from LogicTronix, which is specifically created for enhancing the sharpness of the input image.This IP works by enhancing the input image through a different level of sharpening. Mainly from 50% to 150% of the sharpness level are used for sharpening of the image.This IP can be used on any camera that gives RGB video/image output. The IP supports a maximum of 1920x1080 video resolution. The IP has AXI4-compliant input and output stream interfaces. These interfaces support a 24-bit RGB format.

The IP has an AXI4-Lite Interface which provides better control over the IP. This interface allows setting the video resolution and color output.

Port Description

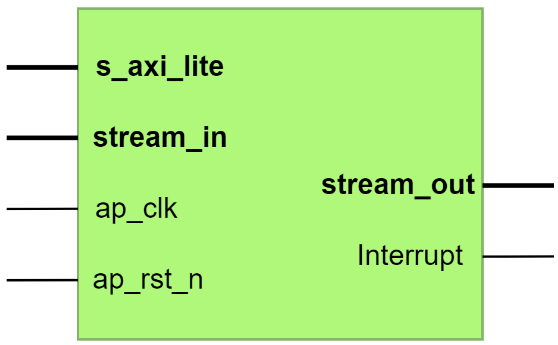

Figure 1. Sharp Enhancement IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow communication with other IPs or system components. The IP core ports are described by the following interfaces.

1. Clock, Reset and Interrupt signal Interface

These signals are summarized in the following table.

Signal Name	Width	Direction	Description
ap_clk	1	IN	Core clock for both AXI4-Stream as well as AXI4-Lite Interface
ap_rst_n	1	IN	Core ap_clk synchronous active low reset
Interrupt	1	OUT	Core Interrupt pin

Table 2. Clock, Reset and Interrupt Signal Interface Description

2. Video Interface

The IP has *stream_in* and *stream_out* interfaces that implement the AXI4-Stream interface protocol. These interfaces are used to get input as well as output stream data respectively.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Signal Name	Width	Direction	Description
AXI4-Stream Input Signals			
stream_in_tdata	24	IN	Input video Data
stream_in_tvalid	1	IN	Input valid
stream_in_tready	1	OUT	Input ready
stream_in_tuser	1	IN	Input video start of frame
stream_in_tlast	1	IN	Input video end of line
stream_in_tstrb	3	IN	Input video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
stream_in_tkeep	3	IN	Input video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
stream_in_tid	1	IN	Input video data identifier
stream_in_tdest	1	IN	Input video data routing information
AXI4-Stream Output Signals			
stream_out_tdata	24	OUT	Output video Data
stream_out_tvalid	1	OUT	Output valid
stream_out_tready	1	IN	Output ready
stream_out_tuser	1	OUT	Output video start of frame
stream_out_tlast	1	OUT	Output video end of line

stream_out_tstrb	3	OUT	Output video data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte
stream_out_tkeep	3	OUT	Output video byte qualifier that indicates whether the content of the associated byte of tdata is processed as part of the data stream
stream_out_tid	1	OUT	Output video data identifier
stream_out_tdest	1	OUT	Output video data routing information

Table 3. AXI4-Stream Signal Names and Descriptions

All streaming interfaces run at *ap_clk*.

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready. INdicates DMA ready to accept the wire address.
s_axi_lite_awaddr	6	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe
s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel. Indicates results of the write transfer

s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready. This indicates the target is ready to receive a response.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready. Indicates DMA is ready to accept the read address.
s_axi_lite_araddr	6	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready. INdicates target is ready to accept the read data.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response. INdicates results of the read transfer.

Table 4. AXI4-Lite Interface Signal Names and Description

This interface also runs at the ap_clk clock.

Register Space

The IP has been generated with built-in registers. These registers must be programmed so that IP can do its job. At the IP hardware level, these registers are accessed by their addresses. These registers are programmed by the AXI4-Lite Interface. When IP software APIs are not available, the IP can be operated by using the register.

The register name, address and description are given below.

BASEADDR Offset (Hex)	Register Name	Type	Description
0x00	Control Signals	R/W	Bit 0: ap_start Bit 1: ap_done Bit 2: ap_idle Bit 3: ap_ready Bit 7: auto_restart
0x04	Global Interrupt Enable Register	R/W	Bit 0: Global Interrupt Enable
0x08	IP Interrupt Enable Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready)
0x0C	IP Interrupt Status Register	R/W	Bit 0: Channel 0 (ap_done) Bit 1: Channel 1 (ap_ready)
0x10	Height	R/W	Number of Active Lines Per Frame
0x18	Width	R/W	Number of active pixels per scanline
0x20	Level	R/W	Sharpness level

Table 5. IP Register Names, Offset Addresses and Descriptions

Video Data

The core generates RGB video data with 1 pixel per clock and 8-bits per component through the *stream_out* port.

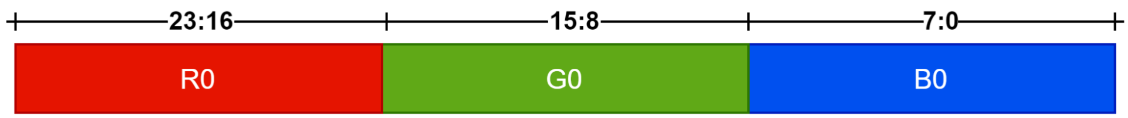

Figure 2. Single Pixel Per Clock, 8-bits per component RGB Video Data Format

Note: Currently IP generates pixel data with 8-bit per color component. However, the IP will be updated to support 10-bit, 12-bit and 16-bit in the future version of IP.

Data Flow

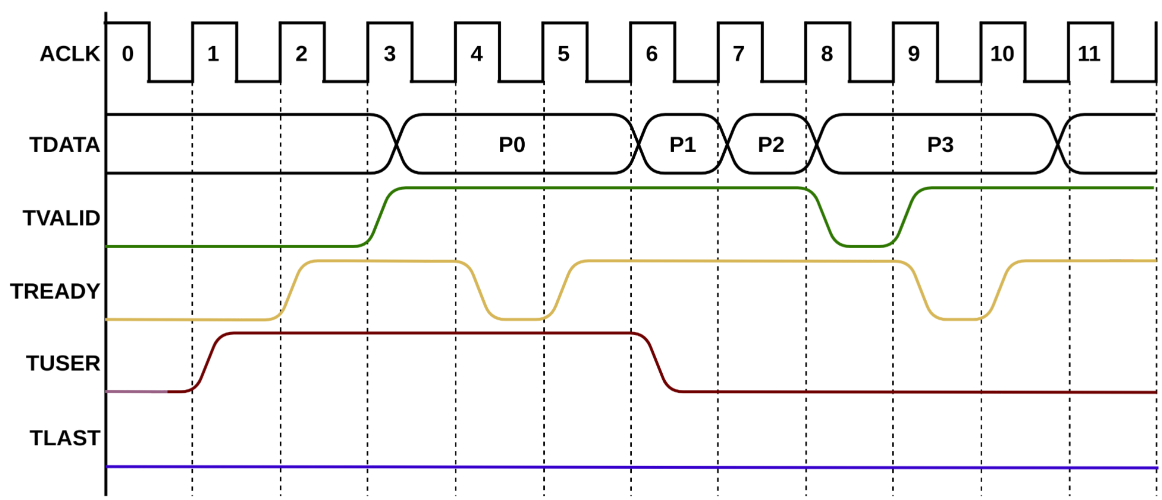

Figure 3. AXI4-Stream Data flow mechanism

The flow of data is according to the AXI4-Stream protocol, which mainly occurs by the four signals in the current IP design. They are; *stream_out_tvalid*, *stream_out_tready*, *stream_out_tuser* (SOF) and *stream_out_tlast* (EOL). These signals are called AXI4-stream handshaking signals. The data is carried out by *stream_out_tdata*.

For a complete transfer of the frame, the SOF signal goes high, which indicates the beginning of the frame. During this moment, *stream_out_tready* and *stream_out_tvalid* must be at HIGH state to begin the flow of valid data from this IP (master) to receiving IP (slave). EOL is asserted HIGH when the transfer of pixels per scanline is completed.

Designing with the SEN IP core

The design with the core has been summarized by the following picture.

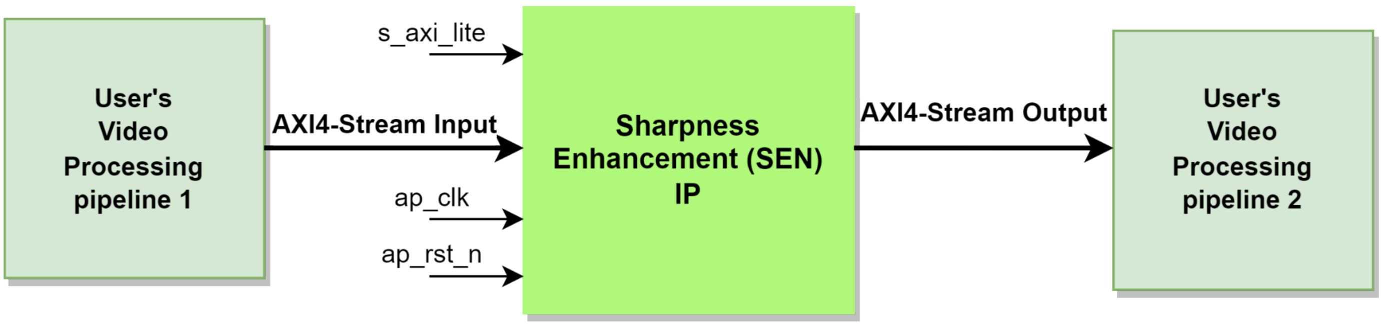

Figure 4. Designing with the Sharp Enhancement IP core

The current version of IP core does not require any IP customization. The core can directly be used in the Vivado IP Integrator.

The IP needs a single clock for both the AXI4-Lite interface and streaming Interface. And the corresponding active low synchronous reset is also required to connect. The IP is configured through the AXI4-Lite interface. Therefore, a software application is required. User has to set the stream resolution.

Performance

Maximum Frequencies

The maximum frequencies that the IP core can be operated on are different due to board types, tool versions and the way of design with the core.

Throughput

As the SEN IP core has input and output AXI4-Stream interfaces, the data throttling is bidirectional. If the source produces valid data and in the meantime, if the destination is ready to receive data, the actual data flow takes place. This flow of data is AXI4-complaint-based.

If *stream_in_tvalid* is not asserted, the SEN core cannot produce valid data for slave IP (destination) and if *stream_out_tready* is not asserted, the core cannot receive valid data from the master IP (source). In this way, if source is producing valid data, indicated by asserting *stream_in_tvalid* HIGH and destination is ready to receive the valid data, indicated by asserting *stream_out_tready* HIGH, the SEN IP core generates the valid data, indicated by asserting *stream_out_tvalid* HIGH. At this moment, the core delivers the 24-bit valid data with one pixel per clock as per *ap_clk*. The core must be operated at least 148.5MHz clock for the 1080p60 resolution.

Resource Utilization

The FPGA resources consumed by Sharp Enhancement IP core is summarized as follows;

Board	Xilinx’s ZYNQ ZC706 Evaluation Board		
Device	xc7z045ffg900-2		
Vivado Version	2019.1		
Resource Utilization			
Site Type	**Available**	**Utilization**	**Utilization %**
Slice	54650	1656	3.03
LUT	218600	4884	2.23
LUTRAM	70400	112	0.16
FF	437200	3842	0.88
DSP	900	22	2.44
BRAM 36K	545	1.5	0.28
BRAM 18K	1090	3	0.28
MMCME2_ADV	8	0	0.00
PLLE2_ADV	8	0	0.00

Table 6. Resource Utilization by Sharp Enhancement core

Example Design

This section provides information about the example design with the core. This example design only consists of a synthesizable design.

Synthesizable Design

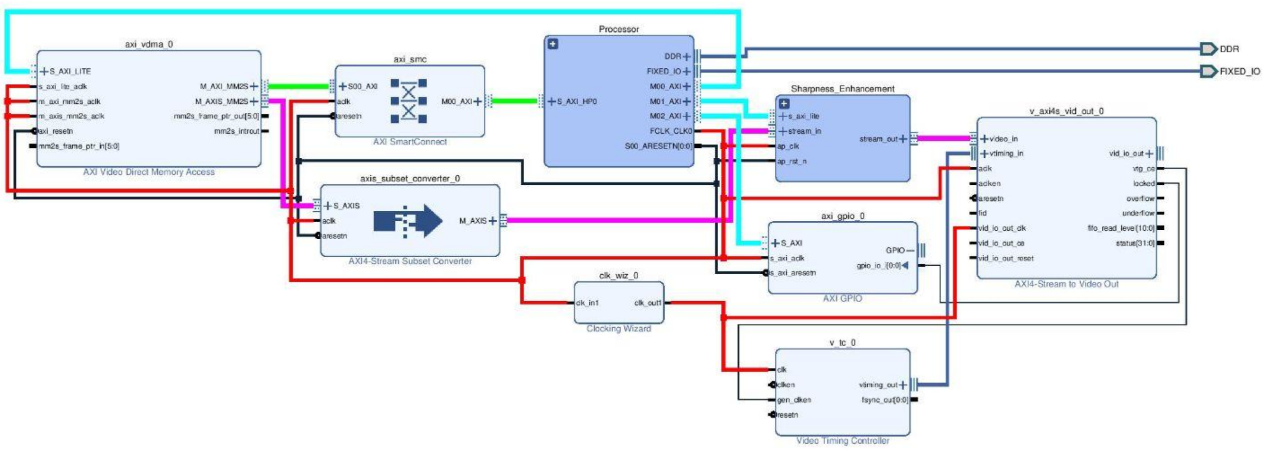

Figure 5. Synthesizable Sharp Enhancement IP core Example Design

The synthesizable example design is shown in the above picture. Please visit the Use Case section to get information about the specific use of the IP core.

Note: This example design is created for the **Xilinx ZC706 Evaluation board**.

This design represents the AXI4-Memory-Mapped based example design. The memory-mapped data of the input image must be loaded into the DDR memory. Memory-mapped-to-Stream (MM2S) conversion is required so that stream data can be given to the SEN IP. For this requirement, VDMA is used with a read channel enabled with 32-bit data width customization. Upon receiving AXI4-Stream as input, the SEN IP core generates a 24-bit sharp enhanced output stream.

The VTC and AXI4-Stream to Video Out are used for outputting the stream in 1080p resolution. However, the output is not passed to the real output device; rather, a locked signal from AXI4-stream to Video Out IP is monitored by an AXI GPIO IP to indicate whether output is obtained successfully or not.

In the SDK part, the layer 1 software APIs are available to initialize and configure the SEN IP core. The API allows to enable or disable interrupt, set stream resolution and sharpness level.

Use Case

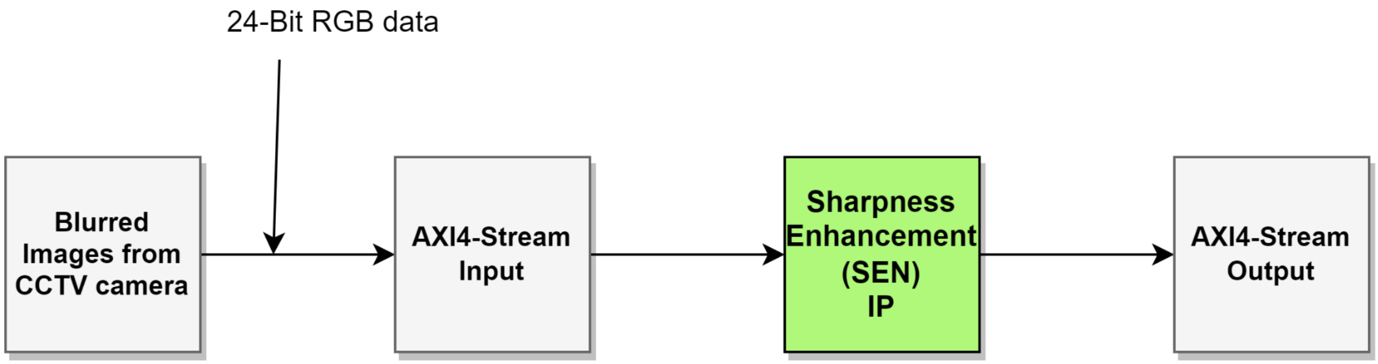

Figure 6. Typical application of Sharp Enhancement IP core

The above picture shows a general use-case of the SEN IP core. In real-life, the sharpness enhancement comes under the post-image enhancement technique. In most CCTV camera sensor interfacing, the sensor does not itself produce well-tuned output images because the quality of the sensor used in most low end CCTV cameras is low which produces blurred images. For such a scenario, several post-image processing algorithms might be required to tune the image perfectly. When sharpness of the image is required, then a sharpness enhancement algorithm comes into play and this is what is achieved by SEN IP. This IP core is a wise choice for FPGA based image processing.

To apply sharp enhancement, the SEN IP core requires AXI4-complaint input image, which means that the camera data needs to be in AXI4-Stream. And oppositely, to get sharp enhanced images displayed, the AXI4-Stream is needed to convert into 24-bit Native Video format.

References

1. Vivado Design Suite: AXI Reference Guide (UG1037)
2. AXI Reference Guide (UG761)
3. Vivado Design Suite User Guide: Designing with IP (UG896)
4. Vivado Design Suite User Guide: Getting Started (UG910)
5. Vivado Design Suite User Guide: Programming and Debugging (UG908)
6. Vivado Design Suite User Guide: Implementation (UG904)

Revision History

The following table shows the revision history of this product guide - PGL038.

Date	Version	Detail
December 28, 2021	1.0	Initial Release

Table 7. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Sharp or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on “Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution”, “Enhancing Financial Trading Algorithms with AI/ML” and “High-Frequency Trading (HFT) based Infrastructure”.

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