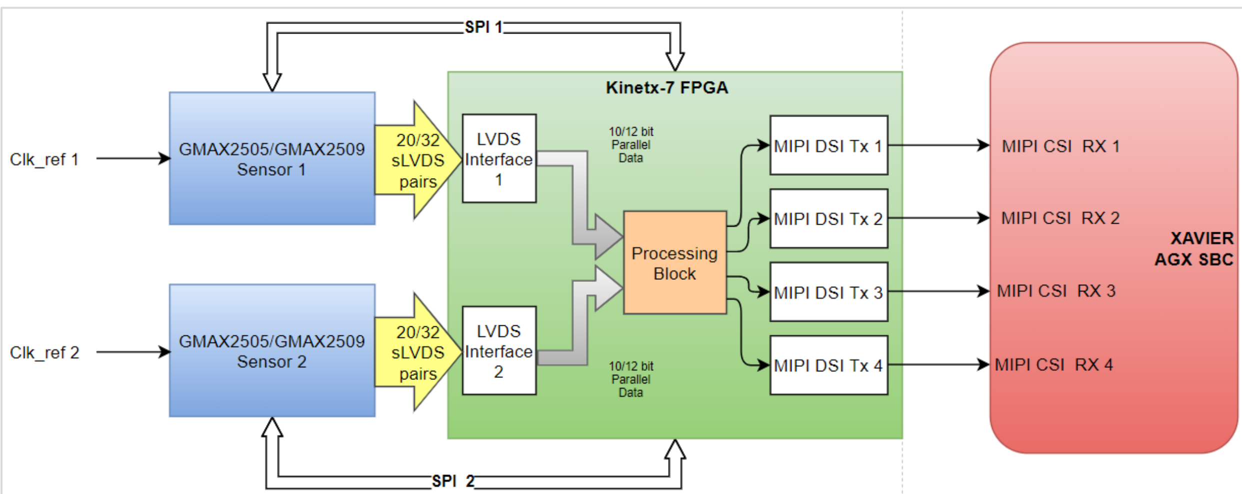
Processing LVDS Camera Stream on FPGA to MIPI DSI Output

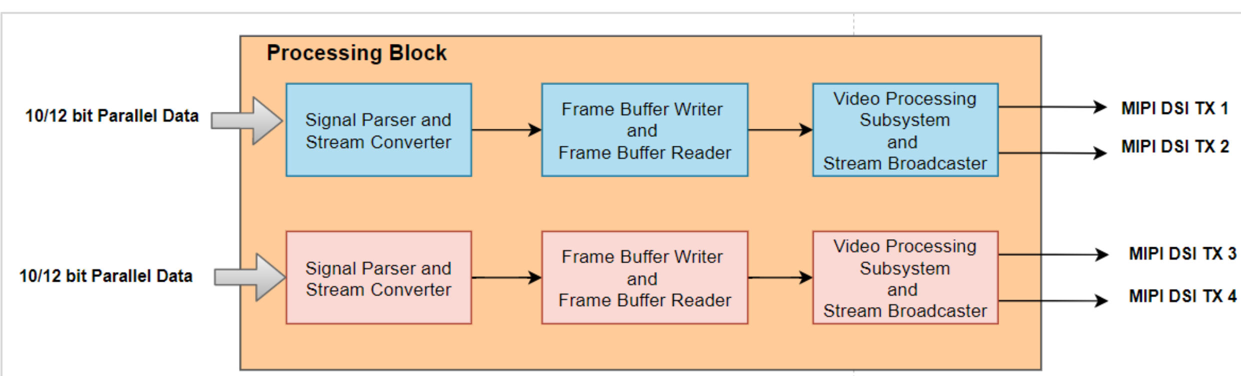
Reference Tutorial

Overview

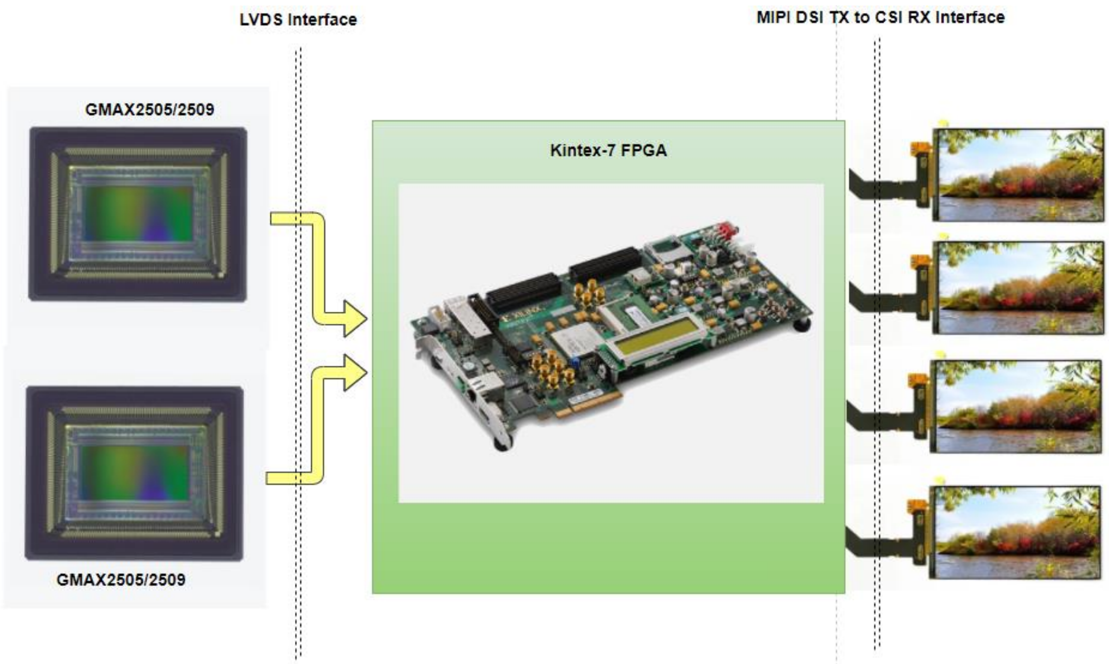
This reference tutorial is on “**Processing High-Speed Camera Stream in FPGA**”. For high speed stream processing **LVDS** (low voltage differential signaling) interface and cameras are highly popular because using LVDS very high stream of captured steam can be transferred or sent to the processing block. In this reference tutorial, we are taking two LVDS CMOS camera sensors from Gpixel and interface those into Xilinx Kintex7 FPGA. The FPGA device perform the stream processing, time synchronizing, pixel binning etc. and creates the MIPI DSI output of 4 MIPI channels.



Fig(a). Functional Diagram of GPixel Sensor sLVDS to DSI design



Fig(b). Expanded Block Diagrammatic View of Processing Block [inside FPGA]



Fig(c). Pictorial Block Diagram (prototyping stage)

Figure(a) shows the functional flow diagram of LVDS into FPGA and then sending it to MIPI DSI format. Figure(b) shows the processing logic which runs inside the FPGA device and Figure(c) shows the top-level prototyping connection between the Gpixel CMOS sensors with FPGA and the MIPI DSI interface.

This LVDS into MIPI processing pipeline consists of mainly three Sections:

1. Camera Input

Two GPixel GMAX2509 cameras are used. The camera specs can be found here; GMAX2509_flyer_EN_2019-11-28.pdf . GMAZ2509 is 4k resolution camera which gives 240+ FPS rate. **This camera is highly used for Machine Vision, High Resolution Industrial Inspection and Intelligent or Smart Traffic Systems**.

GMAX2509 CMOS sensor gives 32 pairs of sLVDS signals. Other variations of camera, such as, GMAX2505 gives 20 pairs of sLVDS signals. In fact, these camera sensors produce

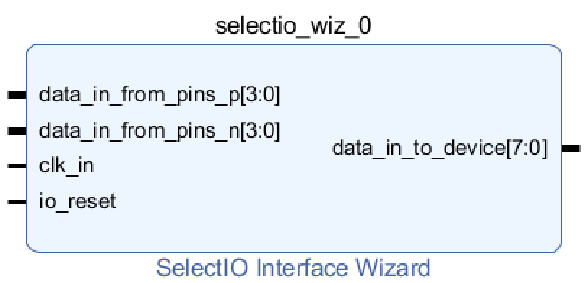
10(GMAX2505)/12 (GMAX2509) bit data. Also, these cameras produce hundreds of frames per second. Using a single-ended signaling standard causes problems to transmit these data to another system. That's why a differential signaling standard is used, which allows to transfer hundreds of frames without losses and interference to another system.

In a nutshell, sLVDS is used to convey the sensor 10/12 bit data to another system with preserved data integrity. Here, the term sLVDS means that sub Low Voltage Differential Signal comes out of GMAX2505/2509 sensor.

In the case of FPGA, there must be such an interface design that can receive those differential signals and parse them into parallel data. When using two cameras altogether, there are 40/64 differential pairs required in the FPGA.

We cannot use general PMOD pins or any bare FPGA pins. Because, LVDS is a pair of signals, which have higher data frequency. Current GPixel camera produces the LVDS signal at maximum 960MHz. On the other hand, PMOD is not made for taking such high-speed data. So, FMC or PMOD pin with differential signaling capabilities is required.

By flowing the Vivado IP Integrator flow, we need **Select I/O Interface Wizard IP**. This helps to interface with various signals, including differential signals like LVDS. This IP is only supported by Zynq-7000, 7-series and 6-series FPGAs. Other IPs might be required for data alignment.



fig(d). Select IO interface Wizard IP, f*or more information, visit Xilinx product guide PG070*

Like the Select I/O interface wizard IP, there is also **High Speed SelectIO Wizard IP**. This only supports Virtex UltraScale+, Kintex UltraScale+, Zynq UltraScale+ MPSoC, Virtex UltraScale and Kintex UltraScale FPGA devices. This IP does not support Vivado IP flow but HDL flow. So, Vivado IP Integrator cannot be used. For the current case, Vivado IP Integrator will be used.
For more information, visit its product guide PG188.

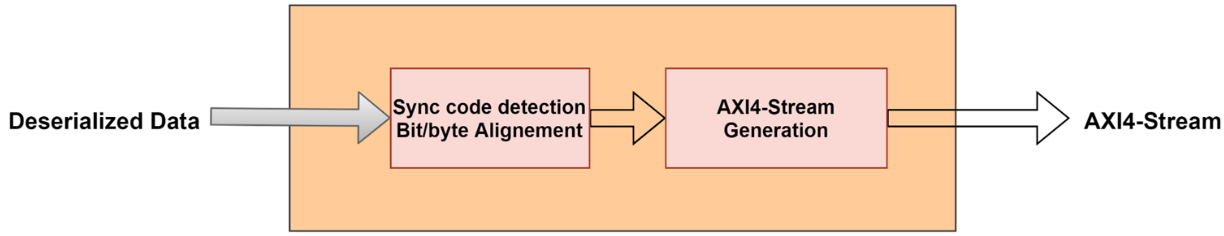
There are also other ways to interface LVDS that such signals can be converted into other forms of signals, like, HDMI, MIPI, VGA, DVI and so on using the LVDS converter tool. But this might turn inefficient.

2. FPGA (Processing Section)

FPGA, as we all know, is a Field Programmable Gate Array. This is in the form of a semiconductor chip, which becomes a major part in this design. All the input interfacing, output interfacing and processing stuff undergo within this chip. Different vendors make FPGA boards using such FPGA chips. Based on the design requirements and complexities, different boards can be selected, for example, 7 Series, UltraScale, UltraScale+ FPGAs and MPSoC FPGA boards can be chosen. The choice of the FPGA must also be dependent on its differential signal receiving capabilities and the MIPI DSI capabilities.
To implement the design upon the FPGA chip, there are two flows, namely, VHDL/Verilog coding flow and Vivado IP Integrator flow. Vivado IP integrator is provided by Xilinx, which enhances the design speed without doing much VHDL/Verilog coding.

For LVDS interfacing, it is required to make deserializer circuit using Xilinx's ISERDES primitives. The deserialized the data have to be aligned with sync code detection to get correct camera data.

The resulting data must be in stream with AXI4-complaint. Once the data is in AXI4-Stream, the different processing, like, object detection, edge detection, color format conversion, video resolution conversion and other video processing things can be done.



Fig(d). Deserialized data into AXI4-Stream

Since there are two GMAX2505/2509 Camera Sensors and each sends the **Sync** signals along with data. Each camera signal has to be processed individually. From the above figure(b), the Signal Parser has to be designed, which can parse sync signals, such as, SOF and EOL for AXI4-Stream handshaking so that AXI4-Stream data can be sent to other processing IPs. Then the data is written to the buffer and read them again for achieving a 60Hz frame rate for down streaming. Finally, after some sort of video processing, the stream can be splitted to transmit a single stream into two MIPI DSI outputs.

From the final project implementation point of view, here are some of the Artix-7 and Kintex-7 FPGA SoM boards by considering their capabilities and prices. We have to make a custom PCB for expanding their interfaces. For their capabilities and prices, the provided links can be visited.

FPGA Device Selection: Table

Trenz Electronic TE0712 FPGA Modules with Xilinx Artix-7

Model	Form factor	FPGA	RAM	SPI Flash	Ethernet	Temperature range
TE0712-02-35-2I	4 x 5 cm	XC7A**35T**-2FGG484I	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	industrial
TE0712-02-42I36-A	4 x 5 cm	XC7A**35T**-2FGG484I	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	industrial
TE0712-02-100-1I	4 x 5 cm	XC7A**100T**-1FGG484I	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	industrial
TE0712-02-71I36-A	4 x 5 cm	XC7A**100T**-1FGG484I	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	industrial
TE0712-02-100-2C	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	commercial
TE0712-02-100-2CA	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3	32 MB MT25QL256ABA8E12	100 Mb	commercial
TE0712-02-72C36-A	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	commercial
TE0712-02-100-2C3 [1)]	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	commercial
TE0712-02-72C36-L [1)]	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3	32 MB S25FL256SAGBHI20	100 Mb	commercial

Trenz Electronic TE0713 FPGA Modules with Xilinx Artix-7

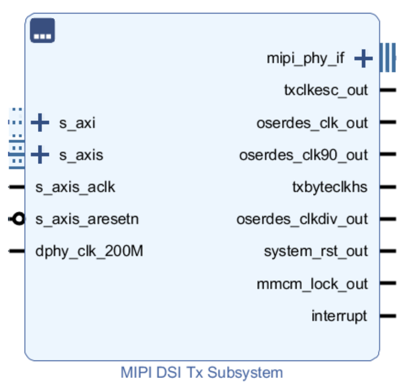
Model	Form factor	FPGA	RAM	Flash	Temperature range
TE0713-02-100-2C	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3L	32 MB S25FL256SAGBHI20	commercial
TE0713-02-72C46-A	4 x 5 cm	XC7A**100T**-2FGG484C	1 GB DDR3L	32 MB S25FL256SAGBHI20	commercial
TE0713-02-200-2C	4 x 5 cm	XC7A**200T**-2FBG484C	1 GB DDR3L	32 MB S25FL256SAGBHI20	commercial
TE0713-02-82C46-A	4 x 5 cm	XC7A**200T**-2FBG484C	1 GB DDR3L	32 MB S25FL256SAGBHI20	commercial

Trenz Electronic TE0741 FPGA Modules with Xilinx Kintex-7

Model	Form factor	FPGA	SPI Flash	Temperature range	Max. GTX transceiver data rate
TE0741-03-070-2CF	4 x 5 cm	XC7K**070T**-2FBG676C	32 MB	commercial	6.6 Gb/s
TE0741-03-070-2IF	4 x 5 cm	XC7K**070T**-2FBG676I	32 MB	industrial	6.6 Gb/s
TE0741-03-160-2CF	4 x 5 cm	XC7K**160T**-2FBG676C	32 MB	commercial	6.6 Gb/s
TE0741-03-160-2C1	4 x 5 cm	XC7K**160T**-2FFG676C	32 MB	commercial	10.3125 Gb/s
TE0741-03-160-2IF	4 x 5 cm	XC7K**160T**-2FBG676I	32 MB	industrial	6.6 Gb/s
TE0741-03-325-2CF	4 x 5 cm	XC7K**325T**-2FBG676C	32 MB	commercial	6.6 Gb/s
TE0741-03-325-2IF	4 x 5 cm	XC7K**325T**-2FBG676I	32 MB	industrial	6.6 Gb/s
TE0741-03-410-2CF	4 x 5 cm	XC7K**410T**-2FBG676C	32 MB	commercial	6.6 Gb/s
TE0741-03-410-2IF	4 x 5 cm	XC7K**410T**-2FBG676I	32 MB	industrial	6.6 Gb/s

3. MIPI DSI output

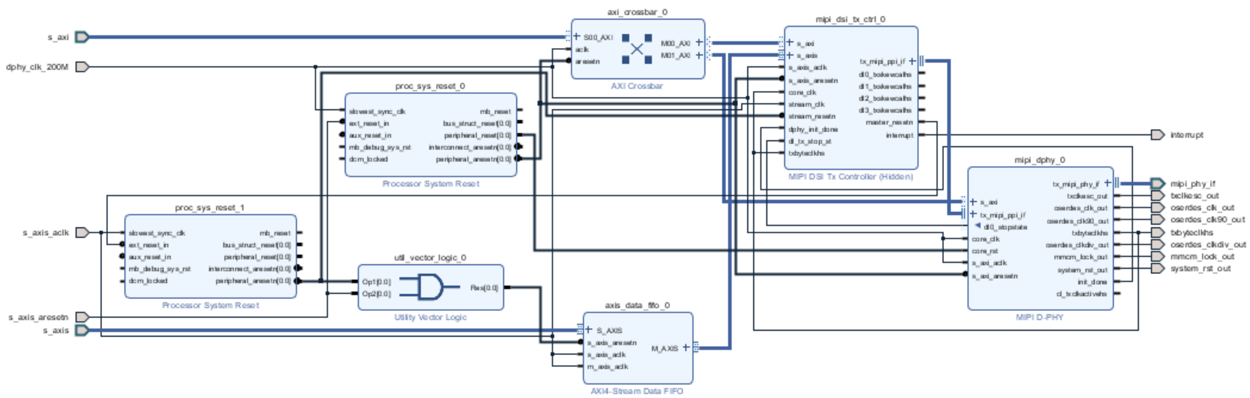
As we all know, unlike MIPI CSI, MIPI DSI, Mobile Industry Peripheral Interface Display Serial Interface, is a high-speed serial interface between a host system and a display module. This produces high-performance, low power and low electromagnetic interference (EMII) while reducing pin count and compatibility across different vendors. It has been widely used such as in mobile, tablets, laptops and other dashboard displays, such as, in car info-tainments and so on.



Fig(e). MIPI DSI Tx Subsystem IP

In the case of FPGA, we have to design this type of interface to display the camera input stream or processed video stream into the display module. Some of the FPGA boards have built-in single

MIPI DSI, which becomes inadequate for this design. The design requirement is to get 4 MIPI DSI output. None of the boards are going to output multiple MIPI DSI but can be designed by using either available FMC pins or creating custom interfaces. If FMC is used, then FMC converter is required.



Fig(f). Subsystems inside MIPI DSI Tx Subsystem IP

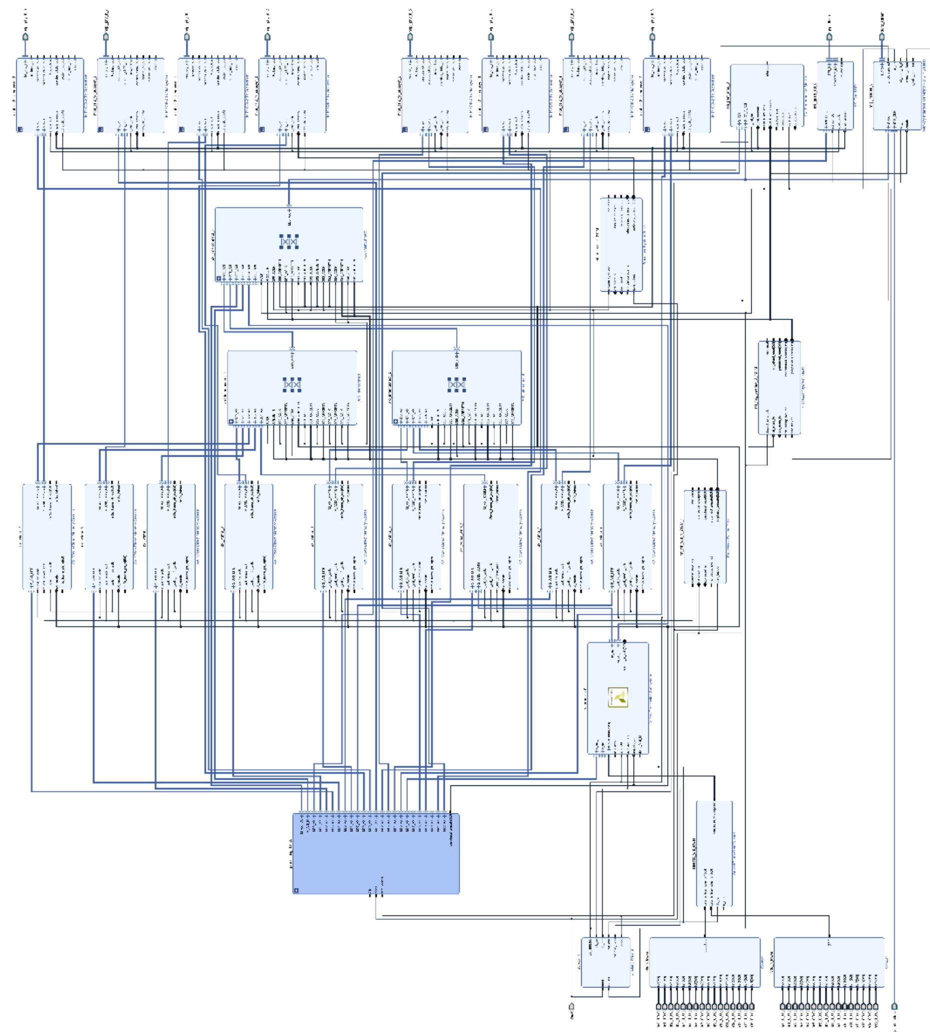
In the design, we use MIPI DSI TX Subsystem IP, as shown in figure(d), which contains other subsystems within it, such as, AXI4-Stream DATA FIFO, MIPI DSI TX controller and MIPI D-PHY. This IP is capable of receiving the video AXI4-Stream and generates frame after marking sync signals in accordance with DSI Protocol and user programmed options. This frame is sent over an MIPI D-PHY transmitter. And then through FPGA pin mapping, the signals are made available to connect other systems, like MIPI CSI. This IP supports 80-2500Mb/s data speed.

For more information, we can visit its product guide PG238.

For the prototyping stage, Sundance FMC-MIPI can be selected from Xilinx [boards-and-kits/1-so55i9], it can support maximum two MIPI DSI, which is also compatible with Virtex UltraScale+, Kintex, UltraScale+, Zynq UltraScale+ MPSoC, Virtex UltraScale, Kintex UltraScale and Zynq-7000.

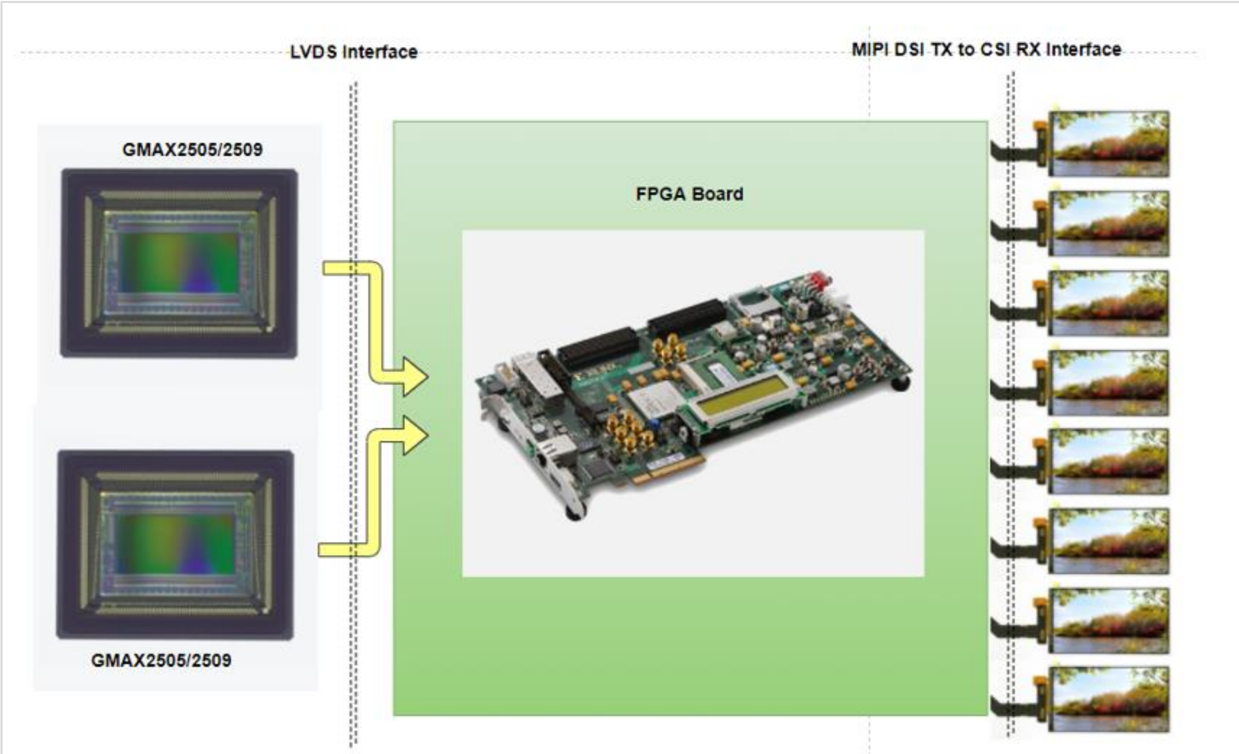
4. Complete VIVADO Block Design

For complete reference design (with VIVADO block design IP Cores and Tcl Script), please write an email to us at: info@logictronix.com .



Fig(g). Complete VIVADO Design for Gpixel-LVDS into MIPI-DSI interfacing

Extended Design [2 LVDS Camera into 8 MIPI DSI]:



Applications and Use Cases:

Reference links:

- Xilinx Application Note [xapp894-d-phy-solutions]
- Xilinx-User Guide [UG471_7Series_SelectIO]
- Meticom[MC20901]
- Xilinx- Application Note xapp524-serial-lvds-adc-interface
- Xilinx-Answer-Record [66786]
- Fastcompression [image-processing]
- Allaboutcircuits [the-why-and-how-of-differential-signaling/]
- Xilinx Answer-Record [50195]
- Xilinx DataSheet [ds182_Kintex_7_Data_Sheet]
- Xilinx DataSheet [ds181_Artix_7_Data_Sheet]
- RS-online [document]
- EEWeb [virtex-7-fpga-data-sheet-dc-and-ac-switching-characteristics/]

For the information about Trenz kintex-7 SoM (TE0741) Variety

- Trenz-Electronic [TE0741-Kintex-7]

About TE0741 TRM, Reference design and others

- Wiki.trenz-electronic

For information about 8-Port SMA / 34 Differential Pair FMC Module (Vita57.1)

- Hitechglobal [FMC_SMA_LVDS]

For variety of Trenz Artix-7 SoM Products

- Trenz-electronic [Programmable-Logic/Xilinx-Artix-7]

For 7-Series Product Guide Selection

- Xilinx-Product-Selection-Guide [7-series-product-selection-guide]

For the VPX3U-XAVIER-SBC module

- VPX3U-XAVIER-SBC_Datasheet

The Impact of Higher Data Rate Requirements on MIPI CSI and MIPI DSI Designs

- NWLogic [mipi-DVCON-Presentation]

Revision History

The following table shows the revision history of this product guide - RFTL013.

Date	Version	Detail
March 23, 2022	1.0	Initial Release

Table 7. IP core Revision History

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution", "Enhancing Financial Trading Algorithms with AI/ML" and "High-Frequency Trading (HFT) based Infrastructure".

For Design Service, IP Cores, Sales and Support: *Contact*

LogicTronix Technologies Pvt. Ltd.

Xilinx Certified Partner & Design Service Partner for Kria SoM for AI/ML

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