

MPSoC Baremetal Training Session- LogicTronix

Session Plan

Total Hours: 20 Hours

Lab Sessions: 7

Objective of Training Session:

1. To familiarize with Kria KV260 and Ultra96v2 Board with projects,
2. Performing the Video pipeline operations with VIVADO/Vitis,
3. Writing SDK applications for **SD read/write, DDR and BRAM,**
4. Using **MIPI CSI-2** sensor interface on Baremetal design flow,
5. Migrating Vivado HLS IP into Vitis HLS,
6. Learning with real world computer vision projects.



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Day 1: 3 hours

Intro:

- Training Session - Content discussion
- MPSoC Device Selection/Architecture
- Familiarization with **Ultra96v2 or Xilinx KV260 board.**

Lab1: Using Display Port to show TPG Stream, and reading File Source (BMP image read) and showing it at display monitor.

- ❖ **Pre:** Brief information about DP. Differentiate with HDMI.
- ❖ **What will be covered in this lab?**
 - ✓ Vivado video pipeline design, streaming and memory mapped designs.
 - ✓ Using or not using **VDMA/ Video Frame buffer Wr/Rd approach**, differentiation between them.
 - ✓ IP Connection discussion, addressing methodologies, PS configurations.
 - ✓ Vitis/SDK coding.

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Day 2: 3 hours

Lab2: Transfer data (Read/Write) between SD Card, DDR, and BRAM.

- ❖ Pre: what will be covered in this lab?
 - Give brief information about the different memories available in the kv260 and ultra96v2 board. Differentiate them. Discussion about Xilinx Fatfile system.

Lab3:

- ❖ Transfer data(Read/Write) between flash, DDR, and BRAM. Also, how to use internal and external flash at the same time?

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Day 3: 4 hours**Lab4:** Interface and configure a Camera Sensor.

- ❖ MIPI, its type, which MIPI type is going to be used in the lab design,
- ❖ what is camera sensor? What is digital Camera Sensor? What kind of sensor is going to be used in this lab? How to program it? What is IIC? Why IIC switch is used? IIC switch address and camera address.
- ❖ The procedure of programming the Camera Sensor.
- ❖ Possible issues and debugging techniques the MIPI designs by checking the registers, ILA debugging method and hardware debugging methods.

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Day 4: 4 hours**Lab5:** Working example of Vitis Vision Library, including software installation on the host machine. (We will share material for software installation prior)

- ❖ Discussion of Vivado hls and Vitis hls.
- ❖ Discussion of design flow in Vitis hls.(Vivado flow and vitis acceleration flow)
- ❖ Migration from Vivado hls to Vitis hls. Libraries discussion, hls_video.h and Vitis vision library. **Example LAB Session on Migration of HLS IP to Vitis Vision.**
- ❖ Why we can't do OpenCV simulation in Vitis HLS like we did in Vivado HLS?
- ❖ Why do we need to install OpenCV in the PC for Vitis HLS OpenCV Simulation.

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Day 5: 4 hours**Lab6:** Write an IP based on Pipelined Streaming I/O using Vitis HLS, allowing continuous processing of data.

- ❖ Streaming based IP designs, such as Crop, Sobel, blur filter, resizing.

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Day 6: 2 hours**Lab7:** Real world project on Ultra96v2 or Kria-KV260

- ❖ Creating MIPI pipeline based design including two or more custom HLS or Vitis HLS IP and sending it to display port as well as saving the frames in the SD card.
- ❖ Objective: to revise all of the completed and learned topics in single project.

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Training Session Requirement:

1. VIVADO 2019.1 (VIVADO/SDK and HLS) and Vitis 2021.1.
2. Ultra96v2 board with mini-DP -HDMI monitor setup. Ultra96v2 UART-JTAG module.
3. Or, Kria KV260 board and Digilent Pcam 5C, this will be used for MIPI based design.
4. Windows or Linux PC (Ubuntu 18.04 or 20.04 preferred) with 8+ Core CPU and 8+ GB RAM.
5. UART terminal program as "GTKterm" or TeraTerm or Putty.
6. 8GB SD card, USB-SD adapter.

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