

Introduction

The CAN FD controller IP core is suited for automotive and general industrial applications. The IP consists of an AXI4-Lite interface which allows easy IP control.

Features

- Designed to ISO 11898-1/2015 [Ref 1]
- Supports CAN and CAN FD frames
- Supports Nominal bit rate up to 1 Mb/s and Data bit rate up to 8 Mb/s
- AXI4-Lite control interface
- TX and RX Mail-Box buffers
- Different modes of operation
 - Configuration Mode
 - Normal Mode
 - Sleep Mode
 - Loopback Mode
 - Bus Monitor Mode
 - One Shot Mode
- Automatic retransmission on error or arbitration loss when the core is not in One Shot Mode

Applications

- Automotive body control units
- Automotive test equipment
- Sensor controls
- Industrial networks

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000
Supported User Interfaces	AXI4-Lite
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Yes
Example Design	Yes
Test Bench	Yes
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

Overview

The CAN FD controller IP is designed to be used in real-time control applications in embedded systems. The IP can be integrated into the target system. It supports both frame formats of CAN and CAN FD.

The IP core has configuration registers and mailbox buffers; TX buffers and RX buffers. The number of mailboxes in the TX buffer and RX buffer are configurable. The TX buffer can be configured up to 32 mailboxes and supports 16 RX mailboxes. Each mailbox at the RX buffer is associated with an Acceptance Filter Mask Register for masking the ID of incoming message frames so that only desired messages are written in the receive message space (see Table 26). The core has 32 Acceptance Filter Code Registers and an Acceptance Filter Code Control Register to control the use of the Code Registers (see Table 20). The RX buffer The registers and message buffers are accessed via the AXI4-Lite interface.

The core starts up in Configuration Mode and can operate in Normal Mode, Sleep Mode, Loopback Mode, and Bus Monitor Mode. While the core is in One-Shot mode, a message will be sent only once, even if there is an arbitration loss or error frame.

Port Description

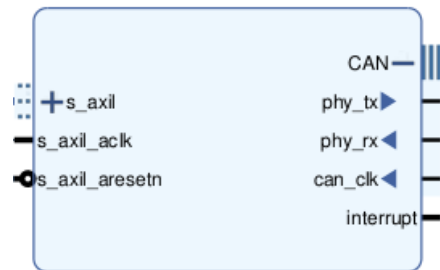


Figure 1. CAN FD IP Top-Level View

The IP is created with industry-standard control and data interfaces. These interfaces allow communication with other IPs or system components. The CAN FD controller core ports are described by the following interfaces.

1. Clock and Reset signal Interface

These signals are summarized in the following table.

Table 2. Clock, Reset Signal Interface Description

Signal Name	Width	Direction	Description
s_axi_clk	1	IN	AXI clock
s_axi_resetn	1	IN	AXI synchronous active low reset
interrupt	1	OUT	Interrupt line

2. CAN Signal Interface

Table 3. CAN Signal Names and Descriptions

Signal Name	Width	Direction	Description
can_clk	1	IN	CAN FD core clock
phy_rx	1	IN	CAN bus RX signal from PHY
phy_tx	1	OUT	CAN bus TX signal to PHY

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface. This allows us to configure or control the IP dynamically. This interface will be connected to Zynq PS or Microblaze.

AXI4-Lite Interface Signals

The AXI4-Lite [\[Ref 2\]](#) Interface signal names and their description are given in the following table.

Table 4. AXI4-Lite Interface Signal Names and Description

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready.
s_axi_lite_awaddr	7	IN	AXI4-Lite Write Address Bus

s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel Write Data Ready.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe
s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel.
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid.
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready.
s_axi_lite_araddr	7	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.
s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response.

Register Space

The IP has specific registers so that IP parameters can be set by accessing these registers and then setting the appropriate hex value. The register can be accessed by its offset address. These registers are programmed by AXI4-Lite Interface.

CAN FD Core Register Address Map

Table 5. CAN FD Core Register Address Map

Address offset	Register Name	Access	Description
0x0000	SRR	R/W	Software Reset Register
0x0004	MSR	R/W	Mode Select Register
0x0008	BRPR	R/W	Arbitration Phase Baud Rate Prescaler Register
0x000C	BTR	R/W	Arbitration Phase Bit Timing Register
0x0010	ECR	R	Error Count Register
0x0014	DP_BRPR	R/W	Data Phase Baud Rate Prescaler
0x0018	DP_BTR	R/W	Data Phase Bit Timing Register
0x000C	BTR	R/W	Arbitration Phase Bit Timing Register
0x0010	ECR	R	Error Count Register
0x0014	DP_BRPR	R/W	Data Phase Baud Rate Prescaler
0x0018	DP_BTR	R/W	Data Phase Bit Timing Register
0x001C	ESR	R/W	Error Status Register
0x0020	SR	R	Status Register
0x0024	ISR	R	Interrupt Status Register
0x0028	IER	R/W	Interrupt Enable Register
0x002C	ICR	R/W	Interrupt Clear Register
0x0030	TRR	R/W	TX Buffer Ready Request Register
0x0034	TCR	R/W	TX Buffer Ready Cancel Request Register
0x0038	ACCR	R/W	Acceptance Filter Code Control Register
0x003C	RXNEMR	R/W	RX Buffer Not Empty Register

0x003C-0x00FF	Reserved	-	Reserved
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CAN FD Core Register Description

1. Software Reset Register; 0x0000

Table 6. Software Reset Register Description

Bits	Name	Access	Reset Value	Description
31:2	Reserved	-	0	Reserved
1	CEN	R/W	0	CAN Enable 1: Enable CAN Core 0: Core in Configuration Mode
0	SRST	R/W	0	Reset 1: resets core Writing 1 to this bit resets the entire CAN FD core including SRR

2. Mode Select Register; 0x0004

Table 7. Mode Select Register Description

Bits	Name	Access	Reset Value	Description
31:5	Reserved	-	0	Reserved
4	OSM	R/W	0	One Shot Mode 1: enables one-shot mode 0: disables one-shot mode When the one-shot mode is enabled, the message frame is transmitted only once ignoring successful or unsuccessful transmission. (This bit can be written only when the CEN bit in SRR is 0)
3	D_BRS	R/W	0	Disable Bit Rate Switch 1: disables the core to transmit CAN FD frames at data bit rate, even if BRS bit at TX message is 1 0: enables the core to transmit CAN FD frames according to the BRS bit in the TX message.

				(This bit can be written only when the CEN bit in SRR is 0)
2	L_BACK	R/W	0	<p>Loopback Mode</p> <p>1: set the core in loopback mode</p> <p>In loopback mode, the core transmits message frames and acknowledges its own transmitted frame. The TX and RX lines are disconnected from outside the core. The core stores the received message as per Acceptance filtering.</p>
1	SLEEP	R/W	0	<p>Sleep Mode</p> <p>1: set the core in sleep mode</p> <p>This bit is cleared when the core wakes up from sleep mode.</p>
0	B_MONITOR	R/W	0	<p>Bus Monitor Mode</p> <p>1: set the core in bus monitor mode</p> <p>The core is in receive only mode, receives messages from the bus and stores in RX buffers as per Acceptance filtering.</p>

3. Arbitration Phase Baud Rate Prescaler Register; 0x0008

Table 8. Arbitration Phase Baud Rate Prescaler Register Description

Bits	Name	Access	Reset Value	Description
31:8	Reserved	-	0	Reserved
7:0	BRP	R/W	0	<p>Arbitration Phase Baud Rate Prescaler</p> <p>Writing these bits sets the baud rate prescaler for the nominal bit rate</p> <p>(These bits can be written only when the CEN bit in SRR is 0)</p>

4. Arbitration Phase Bit Timing Register; 0x000C

Table 9. Arbitration Phase Bit Timing Register Description

Bits	Name	Access	Reset Value	Description
31:23	Reserved	-	0	Reserved
22:16	SJW	R/W	0	Arbitration Phase Synchronization Jump Width Indicates the synchronization jump width for nominal bit timing. SJW is for phase error correction (These bits can be written only when the CEN bit in SRR is 0)
15	Reserved	-	0	Reserved
14:8	TSEG2	R/W	0	Time Segment 2 Indicates the length of phase segment 2 for nominal bit timing. (These bits can be written only when the CEN bit in SRR is 0)
7:0	TSEG1	R/W	0	Time Segment 1 Indicates the sum of the lengths of the propagation segment and phase segment 1 for nominal bit timing. (These bits can be written only when the CEN bit in SRR is 0)

5. Error Count Register; 0x0010

Table 10. Error Count Register Description

Bits	Name	Access	Reset Value	Description
31:16	Reserved	-	0	Reserved
15:8	REC	R	0	RX Error Count Indicates receive error count value. The counter is incremented or decremented as per fault confinement rules defined by the standard. The counter is incremented for every unsuccessful reception. (Writing 1 in SRST bit of SRR clears the count to 0)
7:0	TEC	R	0	TX Error Count

				<p>Indicates transmit error count value. The counter is incremented or decremented as per Fault Confinement rules defined by the standard. The counter is incremented for every unsuccessful transmission. (Writing 1 in SRST bit of SRR clears the count to 0)</p>
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6. Data Phase Baud Rate Prescaler; 0x0014

Table 11. Data Phase Baud Rate Prescaler Register Description

Bits	Name	Access	Reset Value	Description
31:17	Reserved	-	0	Reserved
16	TDC_EN	R/W	0	<p>Transceiver Delay Compensation Enable Indicates TDC enable bit. TDC should be enabled when the data bit rate is more than 2 Mb/s. 1: enables TDC in the core 0: disables TDC in the core (This bit can be written only when the CEN bit in SRR is 0)</p>
15:14	Reserved	-	0	Reserved
13:8	TDC_OFF	R/W		<p>Transceiver Delay Compensation offset Indicates offset value for TDC to locate secondary sample point in data rate in CAN FD. (These bits can be written only when the CEN bit in SRR is 0)</p>
7:0	DP_BRP	R/W	0	<p>Data Phase Baud Rate Prescaler Writing these bits sets the baud rate prescaler for the data bit rate (These bits can be written only when the CEN bit in SRR is 0)</p>

7. Data Phase Bit Timing Register; 0x0018

Table 12. Data Phase Bit Timing Register Description

Bits	Name	Access	Reset Value	Description
31:20	Reserved	-	0	Reserved
19:16	DP_SJW	R/W	0	Data Phase Synchronization Jump Width Indicates the synchronization jump width for data bit timing. (These bits can be written only when the CEN bit in SRR is 0)
15:12	Reserved	-	0	Reserved
11:8	DP_TSEG2	R/W	0	Data Phase Time Segment 2 Indicates the length of phase segment 2 for nominal bit timing. (These bits can be written only when the CEN bit in SRR is 0)
7:5	Reserved	R/W	0	Reserved
4:0	DP_TSEG1	R/W	0	Data Phase Time Segment 1 Indicates the sum of the lengths of the propagation segment and phase segment 1 for data bit timing. (These bits can be written only when the CEN bit in SRR is 0)

8. Error Status Register; 0x001C

Table 13. Error Status Register Description

Bits	Name	Access	Reset Value	Description
31:5	Reserved	-	0	Reserved
4	AERR	R/W	0	ACK Error Indicates an error if the transmitted message has not been acknowledged by any other nodes.. The ack error can occur only when the core is transmitting. 1: Indicates an ack error has occurred 0: Indicates an ack error has not occurred since the bit has been cleared

3	BERR	R/W	0	<p>Bit Error</p> <p>Indicates an error if the sampled bit is different than transmitted. The bit error can occur only when the core is transmitting.</p> <p>1: Indicates a bit error has occurred</p> <p>0: Indicates a bit error has not occurred since the bit has been cleared</p>
2	CERR	R/W	0	<p>CRC Error</p> <p>Indicates an error if the received CRC does not match with the generated CRC in the core</p> <p>1: Indicates a CRC error has occurred</p> <p>0: Indicates a CRC error has not occurred since the bit has been cleared</p>
1	STERR	R/W	0	<p>Stuff Error</p> <p>Indicates an error if bit stuffing is violated.</p> <p>1: Indicates a stuff error has occurred</p> <p>0: Indicates a stuff error has not occurred since the bit has been cleared</p>
0	FMERR	R/W	0	<p>Form Error</p> <p>Indicates an error in the fixed form field violation.</p> <p>1: Indicates a form error has occurred</p> <p>0: Indicates a form error has not occurred since the bit has been cleared</p>

9. Status Register; 0x0020

Table 14. Status Register Description

Bits	Name	Access	Reset Value	Description
31:8	Reserved	-	0	Reserved
7	EACTIVE	R	0 (In unknown state)	<p>Error Active</p> <p>Indicates error state of the core.</p> <p>1: The core is in an error active state.</p> <p>0: The core is not in an error active state.</p>
6	EPASSIVE	R	0	<p>Error Passive</p> <p>Indicates error state of the core.</p> <p>1: The core is in an error passive state.</p>

				0: The core is not in an error passive state.
5	BUS_OFF	R	0	Bus Off Indicates error status of the core. 1: The core is in a bus off-state. 0: The core is not in a bus-off state.
4	LBACK_S	R	0	Loopback Mode Status Indicates the current mode of the core. 1: The core is in loopback mode 0: The core is not in loopback mode.
3	B_MONITOR_S	R	0	Bus Monitor Mode Status Indicates the current mode of the core. 1: The core is in bus monitor mode. 0: The core is not in bus monitor mode
2	SLEEP_S	R	0	Sleep Mode Status Indicates the current mode of the core 1: The core is in sleep mode. 0: The core is not in sleep mode.
1	NORM_S	R	0	Normal Mode Status Indicates the current mode of the core. 1: The core is in normal mode. 0: The core is not in normal mode.
0	CONFIG_S	R	1	Configuration Mode Status Indicates the current mode of the core. 1: The core is in configuration mode. 0: The core is not in configuration mode.

10. Interrupt Status Register; 0x0024

Table 15. Interrupt Status Register Description

Bits	Name	Access	Reset Value	Description
31:10	Reserved	-	0	Reserved
9	BSOFF_RECOV	R	0	Bus Off Recovered Interrupt 1: Indicates the core recovered from the bus off-state. The core entered an error active state from the bus off state.
8	BSOFF	R	0	Bus Off Interrupt 1: Indicates the core entered in the bus off-state.
7	RX_S	R	0	Reception Success Interrupt

				1: Indicates the message frame was successfully received by the core.
6	SLEEP	R	0	Seep Interrupt 1: Indicates the core entered sleep mode.
5	WAKEUP	R	0	Wake Up Interrupt 1: Indicates the core entered normal mode from sleep mode.
4	TXCS	R	0	Transmission Cancel Served Interrupt 1: Indicates transmission cancel request has been accepted and served.
3	TXRS	R	0	Transmission Request Served Interrupt 1: Indicates the buffer ready request (TRR) has been accepted and served.
2	ERROR	R		Error Interrupt 1: Indicates an error has occurred.
1	TX_S	R	0	Transmission Success Interrupt 1: Indicates the message has been successfully transmitted.
0	ARBLOSS	R	0	Arbitration Loss Interrupt 1: Indicates the arbitration was lost during message transmission.

11. Interrupt Enable Register; 0x0028

Table 16. Interrupt Enable Register Description

Bits	Name	Access	Reset Value	Description
31:10	Reserved	-	0	Reserved
9	E_BSOFF_R ECOV	R/W	0	Bus Off Recovered Interrupt Enable 1: Enables interrupt generation if BSOFF_RECOV bit in ISR is set. 0: Disables interrupt generation if BSOFF_RECOVbit in ISR is set.
8	E_BSOFF	R/W	0	Bus Off Interrupt Enable 1: Enables interrupt generation if The BSOFF bit in ISR is set. 0: Disables interrupt generation if

				The BSOFF bit in ISR is set.
7	E_RX_S	R/W	0	Reception Success Interrupt Enable 1: Enables interrupt generation if RX_S bit in ISR is set. 0: Disables interrupt generation if RX_S bit in ISR is set.
6	E_SLEEP	R/W	0	Seep Interrupt Enable 1: Enables interrupt generation if the SLEEP bit in ISR is set. 0: Disables interrupt generation if the SLEEP bit in ISR is set.
5	E_WAKEUP	R/W	0	Wake Up Interrupt Enable 1: Enables interrupt generation if the WAKEUP bit in ISR is set. 0: Disables interrupt generation if the WAKEUP bit in ISR is set.
4	E_TXCS	R/W	0	Transmission Cancel Served Interrupt Enable 1: Enables interrupt generation if TXCS bit in ISR is set. 0: Disables interrupt generation if TXCS bit in ISR is set.
3	E_TXRS	R/W	0	Transmission Request Served Interrupt Enable 1: Enables interrupt generation if TXRS bit in ISR is set. 0: Disables interrupt generation if TXRS bit in ISR is set.
2	E_ERROR	R/W		Error Interrupt Enable 1: Enables interrupt generation if ERROR bit in ISR is set. 0: Disables interrupt generation if ERROR bit in ISR is set.
1	E_TX_S	R/W	0	Transmission Success Interrupt Enable 1: Enables interrupt generation if TX_S bit in ISR is set. 0: Disables interrupt generation if TX_S bit in ISR is set.
0	E_ARBLOSS	R/W	0	Arbitration Loss Interrupt Enable 1: Enables interrupt generation if ARBLOSS bit in ISR is set. 0: Disables interrupt generation if ARBLOSS bit in ISR is set.

12. Interrupt Clear Register; 0x002C
Table 17. Interrupt Clear Register Description

Bits	Name	Access	Reset Value	Description
31:10	Reserved	-	0	Reserved
9	C_BSOFF_R ECOV	W	0	Bus Off Recovered Interrupt 1: Clears Bus Off Recovered Interrupt status bit.
8	C_BSOFF	W	0	Bus Off Interrupt 1: Clears Bus Off Interrupt status bit.
7	C_RX_S	W	0	Reception Success Interrupt 1: Clears Reception Success Interrupt status bit.
6	C_SLEEP	W	0	Seep Interrupt 1: Clears Sleep Interrupt status bit.
5	C_WAKEUP	W	0	Wake Up Interrupt 1: Wake Up Interrupt status bit.
4	C_TXCS	W	0	Transmission Cancel Served Interrupt 1: Clears Transmission Cancel Served Interrupt status bit.
3	C_TXRS	W	0	Transmission Request Served Interrupt 1: Clears Transmission Request Served Interrupt status bit.
2	C_ERROR	W		Error Interrupt 1: Clears Error Interrupt status bit.
1	C_TX_S	W	0	Transmission Success Interrupt Clear 1: Clears Transmission Success Interrupt status bit.
0	C_ARBLOSS	W	0	Arbitration Loss Interrupt Clear 1: Clears Arbitration Loss Interrupt status bit.

13. TX buffer Ready Request Register; 0x0030

Table 18. TX Buffer Ready Request Register Description

Bits	Name	Access	Reset Value	Description
31:8	RR31/RR8	R/W	0	TX Buffer Ready Request Register of buffer 31 to 8 These bits exist based on the number of TX buffers.
7	RR7	R/W	0	TX Buffer 7 Ready Request Register 1: TX Buffer 7 is ready for transmission.
6	RR6	R/W	0	TX Buffer 6 Ready Request Register 1: TX Buffer 6 is ready for transmission.
5	RR5	R/W	0	TX Buffer 5 Ready Request Register 1: TX Buffer 5 is ready for transmission.
4	RR4	R/W	0	TX Buffer 4 Ready Request Register 1: TX Buffer 4 is ready for transmission.
3	RR3	R/W	0	TX Buffer 3 Ready Request Register 1: TX Buffer 3 is ready for transmission.
2	RR2	R/W	0	TX Buffer 2 Ready Request Register 1: TX Buffer 2 is ready for transmission.
1	RR1	R/W	0	TX Buffer 1 Ready Request Register 1: TX Buffer 1 is ready for transmission.
0	RR0	R/W	0	TX Buffer 0 Ready Request Register 1: TX Buffer 0 is ready for transmission.

14. TX buffer Cancel Request Register; 0x0034

Table 19. TX Buffer Cancel Request Register Description

Bits	Name	Access	Reset Value	Description
31:8	CR31/CRR8	R/W	0	TX Buffer Cancel Request Register of buffer 31 to 8 These bits exist based on the number of TX buffers.
7	CR7	R/W	0	TX Buffer 7 Cancel Request Register

6	CR6	R/W	0	TX Buffer 6 Cancel Request Register
5	CR5	R/W	0	TX Buffer 5 Cancel Request Register
4	CR4	R/W	0	TX Buffer 4 Cancel Request Register
3	CR3	R/W	0	TX Buffer 3 Cancel Request Register
2	CR2	R/W	0	TX Buffer 2 Cancel Request Register
1	CR1	R/W	0	TX Buffer 1 Cancel Request Register
0	CR0	R/W	0	TX Buffer 0 Cancel Request Register

15. Acceptance Filter Code Control Register; 0x0038

Table 20. Acceptance Filter Code Control Register Description

Bits	Name	Access	Reset Value	Description
31	UAFCR32	R/W	0	Use Acceptance Filter Code Register 31 1: Indicates the Acceptance Filter Code Register 31 is used for acceptance filtering.
30	UAFCR30	R/W	0	Use Acceptance Filter Code Register 30 1: Indicates the Acceptance Filter Code Register 30 is used for acceptance filtering.
29	UAFCR29	R/W	0	Use Acceptance Filter Code Register 29 1: Indicates the Acceptance Filter Code Register 29 is used for acceptance filtering.
28	UAFCR28	R/W	0	Use Acceptance Filter Code Register 28 1: Indicates the Acceptance Filter Code Register 28 is used for acceptance filtering.
27	UAFCR27	R/W	0	Use Acceptance Filter Code Register 27 1: Indicates the Acceptance Filter Code Register 27 is used for acceptance filtering.
26	UAFCR26	R/W	0	Use Acceptance Filter Code Register 26 1: Indicates the Acceptance Filter Code Register 26 is used for acceptance filtering.

25	UAFCR25	R/W	0	Use Acceptance Filter Code Register 25 1: Indicates the Acceptance Filter Code Register 25 is used for acceptance filtering.
24	UAFCR24	R/W	0	Use Acceptance Filter Code Register 24 1: Indicates the Acceptance Filter Code Register 24 is used for acceptance filtering.
23	UAFCR23	R/W	0	Use Acceptance Filter Code Register 23 1: Indicates the Acceptance Filter Code Register 23 is used for acceptance filtering.
22	UAFCR22	R/W	0	Use Acceptance Filter Code Register 22 1: Indicates the Acceptance Filter Code Register 22 is used for acceptance filtering.
21	UAFCR21	R/W	0	Use Acceptance Filter Code Register 21 1: Indicates the Acceptance Filter Code Register 21 is used for acceptance filtering.
20	UAFCR20	R/W	0	Use Acceptance Filter Code Register 20 1: Indicates the Acceptance Filter Code Register 20 is used for acceptance filtering.
19	UAFCR19	R/W	0	Use Acceptance Filter Code Register 19 1: Indicates the Acceptance Filter Code Register 19 is used for acceptance filtering.
18	UAFCR18	R/W	0	Use Acceptance Filter Code Register 18 1: Indicates the Acceptance Filter Code Register 18 is used for acceptance filtering.
17	UAFCR17	R/W	0	Use Acceptance Filter Code Register 17 1: Indicates the Acceptance Filter Code Register 17 is used for acceptance filtering.
16	UAFCR16	R/W	0	Use Acceptance Filter Code Register 16 1: Indicates the Acceptance Filter Code Register 16 is used for acceptance filtering.
15	UAFCR15	R/W	0	Use Acceptance Filter Code Register 15 1: Indicates the Acceptance Filter Code Register 15 is used for acceptance filtering.
14	UAFCR14	R/W	0	Use Acceptance Filter Code Register 14 1: Indicates the Acceptance Filter Code Register 14 is used for acceptance filtering.
13	UAFCR13	R/W	0	Use Acceptance Filter Code Register 13 1: Indicates the Acceptance Filter Code Register 13 is used for acceptance filtering.

12	UAFCR12	R/W	0	Use Acceptance Filter Code Register 12 1: Indicates the Acceptance Filter Code Register 12 is used for acceptance filtering.
11	UAFCR11	R/W	0	Use Acceptance Filter Code Register 11 1: Indicates the Acceptance Filter Code Register 11 is used for acceptance filtering.
10	UAFCR10	R/W	0	Use Acceptance Filter Code Register 10 1: Indicates the Acceptance Filter Code Register 10 is used for acceptance filtering.
9	UAFCR9	R/W	0	Use Acceptance Filter Code Register 9 1: Indicates the Acceptance Filter Code Register 9 is used for acceptance filtering.
8	UAFCR8	R/W	0	Use Acceptance Filter Code Register 8 1: Indicates the Acceptance Filter Code Register 8 is used for acceptance filtering.
7	UAFCR7	R/W	0	Use Acceptance Filter Code Register 7 1: Indicates the Acceptance Filter Code Register 7 is used for acceptance filtering.
6	UAFCR6	R/W	0	Use Acceptance Filter Code Register 6 1: Indicates the Acceptance Filter Code Register 6 is used for acceptance filtering.
5	UAFCR5	R/W	0	Use Acceptance Filter Code Register 5 1: Indicates the Acceptance Filter Code Register 5 is used for acceptance filtering.
4	UAFCR4	R/W		Use Acceptance Filter Code Register 4 1: Indicates the Acceptance Filter Code Register 4 is used for acceptance filtering.
3	UAFCR3	R/W	0	Use Acceptance Filter Code Register 3 1: Indicates the Acceptance Filter Code Register 3 is used for acceptance filtering.
2	UAFCR2	R/W		Use Acceptance Filter Code Register 2 1: Indicates the Acceptance Filter Code Register 2 is used for acceptance filtering.
1	UAFCR1	R/W	0	Use Acceptance Filter Code Register 1 1: Indicates the Acceptance Filter Code Register 1 is used for acceptance filtering.
0	UAFCR0	R/W	0	Use Acceptance Filter Code Register 0 1: Indicates the Acceptance Filter Code Register 0 is used for acceptance filtering.

16. RX buffer Not Empty Register; 0x003C
Table 21. RX Buffer Not Empty Register Description

Bits	Name	Access	Reset Value	Description
31:16	Reserved	-	0	Reserved
15:8	RXNEM15 - RXNEM8	R/W	0	RX Buffer 15 Not Empty to RX Buffer 8 Not Empty Writing value 1 in these bits clears the bits.
7	RXNEM7	R/W	0	RX Buffer 7 Not Empty Writing value 1 in this bit clears the bit.
6	RXNEM6	R/W	0	RX Buffer 6 Not Empty Writing value 1 in this bit clears the bit.
5	RXNEM5	R/W	0	RX Buffer 5 Not Empty Writing value 1 in this bit clears the bit.
4	RXNEM4	R/W	0	RX Buffer 4 Not Empty Writing value 1 in this bit clears the bit.
3	RXNEM3	R/W	0	RX Buffer 3 Not Empty Writing value 1 in this bit clears the bit.
2	RXNEM2	R/W	0	RX Buffer 2 Not Empty Writing value 1 in this bit clears the bit.
1	RXNEM1	R/W	0	RX Buffer 1 Not Empty Writing value 1 in this bit clears the bit.
0	RXNEM0	R/W	0	RX Buffer 0 Not Empty Writing value 1 in this bit clears the bit.

TX Message Register Space

TX Message Register (Mailbox) Address Map

Table 22. TX Message Register Description

Address offset	Register Name	Access	Description
0x0100	TB0-ID	R/W	TB ID Register
0x0104	TB0-DLC	R/W	TB DLC Register
0x0108	TB0-DW0	R/W	Data Words
0x010C	TB0-DW1	R/W	
0x0110	TB0-DW2	R/W	
0x0114	TB0-DW3	R/W	
0x0118	TB0-DW4	R/W	
0x011C	TB0-DW5	R/W	
0x0120	TB0-DW6	R/W	
0x0124	TB0-DW7	R/W	
0x0128	TB0-DW8	R/W	
0x012C	TB0-DW9	R/W	
0x0130	TB0-DW10	R/W	
0x0134	TB0-DW11	R/W	
0x0138	TB0-DW12	R/W	
0x013C	TB0-DW13	R/W	
0x0140	TB0-DW14	R/W	
0x0144	TB0-DW15	R/W	
Address Map of TX buffer 1 to TX buffer 7			
0x0148- 0x018C	TB1	R/W	TX Buffers
0x0190-	TB2	R/W	

Address offset	Register Name	Access	Description
0x01D4			TX Buffers
0x01D8-0x021C	TB3	R/W	
0x0220-0x0264	TB4	R/W	
0x0268-0x02AC	TB5	R/W	
0x02B0-0x02F4	TB6	R/W	
0x02F8-0x033C	TB7	R/W	
Address Map of TX buffer 8 to TX buffer 15			
0x0340-0x0384	TB8	R/W	TX Buffers
0x0388-0x03CC	TB9	R/W	
0x03D0-0x0414	TB10	R/W	
0x0418-0x045C	TB11	R/W	
0x0460-0x04A4	TB12	R/W	
0x04A8-0x04EC	TB13	R/W	
0x04F0-0x0534	TB14	R/W	
0x0538-0x057C	TB15	R/W	
Address Map of TX buffer 16 to TX buffer 31			
0x0580-0x05C4	TB16	R/W	TX Buffers
0x05C8-	TB17	R/W	

Address offset	Register Name	Access	Description
0x060C			
0x0610-0x0654	TB18	R/W	TX Buffers
0x0658-0x069C	TB19	R/W	
0x06A0-0x06E4	TB20	R/W	
0x06E8-0x072C	TB21	R/W	
0x0730-0x0774	TB22	R/W	
0x0778-0x07BC	TB23	R/W	
0x07C0-0x0804	TB24	R/W	
0x0808-0x084C	TB25	R/W	
0x0850-0x0894	TB26	R/W	
0x0898-0x08DC	TB27	R/W	
0x08E0-0x0934	TB28	R/W	
0x0928-0x096C	TB29	R/W	
0x0970-0x09B4	TB30	R/W	
0x09B8-0x09FC	TB31	R/W	
Acceptance Filter Code Registers			
0x0A00	ACR0	R/W	Acceptance Filter Code Register 0
0x0A04	ACR1	R/W	Acceptance Filter Code Register 1

Address offset	Register Name	Access	Description
0x0A08	ACR2	R/W	Acceptance Filter Code Register 2
0x0A0C	ACR3	R/W	Acceptance Filter Code Register 3
0x0A10	ACR4	R/W	Acceptance Filter Code Register 4
0x0A14	ACR5	R/W	Acceptance Filter Code Register 5
0x0A18	ACR6	R/W	Acceptance Filter Code Register 6
0x0A1C	ACR7	R/W	Acceptance Filter Code Register 7
0x0A20	ACR8	R/W	Acceptance Filter Code Register 8
0x0A24	ACR9	R/W	Acceptance Filter Code Register 9
0x0A28	ACR10	R/W	Acceptance Filter Code Register 10
0x0A2C	ACR12	R/W	Acceptance Filter Code Register 12
0x0A30	ACR11	R/W	Acceptance Filter Code Register 11
0x0A34	ACR13	R/W	Acceptance Filter Code Register 13
0x0A38	ACR14	R/W	Acceptance Filter Code Register 14
0x0A3C	ACR15	R/W	Acceptance Filter Code Register 15
0x0A40	ACR16	R/W	Acceptance Filter Code Register 16
0x0A54	ACR17	R/W	Acceptance Filter Code Register 17
0x0A58	ACR18	R/W	Acceptance Filter Code Register 18
0x0A5C	ACR19	R/W	Acceptance Filter Code Register 19
0x0A60	ACR20	R/W	Acceptance Filter Code Register 20
0x0A64	ACR21	R/W	Acceptance Filter Code Register 21
0x0A68	ACR22	R/W	Acceptance Filter Code Register 22
0x0A6C	ACR23	R/W	Acceptance Filter Code Register 23
0x0A70	ACR24	R/W	Acceptance Filter Code Register 24
0x0A74	ACR25	R/W	Acceptance Filter Code Register 25
0x0A78	ACR26	R/W	Acceptance Filter Code Register 26

Address offset	Register Name	Access	Description
0x0A7C	ACR27	R/W	Acceptance Filter Code Register 27
0x0A80	ACR28	R/W	Acceptance Filter Code Register 28
0x0A84	ACR29	R/W	Acceptance Filter Code Register 29
0x0A88	ACR30	R/W	Acceptance Filter Code Register 30
0x0A8C	ACR31	R/W	Acceptance Filter Code Register 31

TX Message Register Description

1. TX Message ID Register

Table 23. TX Message ID Register Description

Bits	Name	Access	Reset Value	Description
31:21	BID	R/W	0	Standard Message ID. The base ID (11 bits) of the frame in Base Format.. This field is valid for both CAN and CAN FD standard and extended frames.
20	SRR	R/W	0	Substitute Remote Transmission Request. 1: Indicates the message is a Remote Frame in CAN Base Format. 0: Indicates the message is Data Frame in CAN Base Format. This bit is valid only for the Base formats of CAN and CAN

				FD. For extended formats, the bit should be set to 1.
19	IDE	R/W	0	Identifier Extension 1: Indicates the message frame is in Extended Format. 0: Indicates the message frame is in Base Format.
18:1	EXID	R/W	0	Extended ID The extended identifier(18 bits) of the message frame. This field is valid only for Extended Format Frames in CAN and CAN FD.
0	RTR	R/W	0	Remote Transmission Request 1: Indicates the message is a Remote Frame in CAN Extended Format. 0: Indicates the message is Data Frame in CAN Extended Format. This bit is valid only for Extended formats of CAN and CAN FD. For standard formats the bit should be set 0.

2. TX Message DLC Register

Table 24. TX Message DLC Register Description

Bits	Name	Access	Reset Value	Description
31:28	DLC	R/W	0	Data Length Code. Indicates the data length code of the control field of the CAN and CAN FD message frame. The value is in the number of bytes.
27	EDL/.FDF	R/W	0	Extended Data Length/FD Frame Format 1: Indicates CAN FD message frame. 0: Indicates the CAN message frame.
26	BRS	R/W	0	Bit Rate Switch This bit decides whether the bit rate is switched inside a CAN FD frame format frame or not. 1: Bit rate is switched from nominal to data bit rate. 0: The bit rate is not switched.
25:0	Reserved	-	0	Reserved

3. TX Message Data Word 0 (DW0) Register

Table 25. TX Message Data word Register Description

Bits	Name	Access	Reset Value	Description
31:24	DB0	R/W	0	Data Byte 0
23:16	DB1	R/W	0	Data Byte 1
15:8	DB2	R/W	0	Data Byte 2
7:0	DB3	R/W	0	Data Byte 3

4. Acceptance Filter Code Register (ACR*)

Table 26. Acceptance Filter Code Register Description

Bits	Name	Access	Reset Value	Description
31:21	BID_ACR	R/W	0	Standard Message ID ACR. If the corresponding bits at Mask Register RB*_AMR is 1, the message that has a BID equivalent to the bits in this field is accepted and stored in the RX buffer.
20	SRR_ACR	R/W	0	Substitute Remote Transmission Request ACR. If the corresponding bit at Mask Register RB*_AMR is 1, 1: Stores standard remote CAN frame only. 0: Stores standard data CAN frame only.
19	IDE_ACR	R/W	0	Identifier Extension ACR. If the corresponding bit at Mask Register RB*_AMR is 1, 1: Stores extended CAN and CAN FD message frames only. 0: Stores standard CAN and CAN FD message frames only.
18:1	EXID_ACR	R/W	0	Extended ID ACR. If the corresponding bits at Mask Register RB*_AMR is 1, the message that has an EXID equivalent to the bits in this field is accepted and stored in the RX buffer.
0	RTR_ACR	R/W	0	Remote Transmission Request ACR. If the corresponding bit at Mask Register RB*_AMR is 1, 1: Stores CAN remote frame messages only. 0: Stores CAN data frame messages only.

RX Message Register Space

RX Message Register (Mailbox) Address Map

Table 27. RX Message Register Description

Address offset	Register Name	Access	Description
0x2100	RB0-ID	R	RB ID Register
0x2104	RB0-DLC	R	RB DLC Register
0x2108	RB0-DW0	R	Received Frame Data Words
0x210C	RB0-DW1	R	
0x2110	RB0-DW2	R	
0x2114	RB0-DW3	R	
0x2118	RB0-DW4	R	
0x211C	RB0-DW5	R	
0x2120	RB0-DW6	R	
0x2124	RB0-DW7	R	
0x2128	RB0-DW8	R	
0x212C	RB0-DW9	R	
0x2130	RB0-DW10	R	
0x2134	RB0-DW11	R	
0x2138	RB0-DW12	R	
0x213C	RB0-DW13	R	
0x2140	RB0-DW14	R	
0x2144	RB0-DW15	R	
Address Map of RX Buffer 1 to RX Buffer 7			
0x2148- 0x218C	RB1	R	
0x2190-	RB2	R	

0x21D4			RX Buffers
0x21D8-0x221C	RB3	R	
0x2220-0x2264	RB4	R	
0x2268-0x22AC	RB5	R	
0x22B0-0x22F4	RB6	R	
0x22F8-0x233C	RB7	R	
Address Map of RX Buffer 8 to RX Buffer 15			
0x2340-0x2384	RB8	R	RX Buffers
0x2388-0x23CC	RB9	R	
0x23D0-0x2414	RB10	R	
0x2418-0x245C	RB11	R	
0x2460-0x24A4	RB12	R	
0x24A8-0x24EC	RB13	R	
0x24F0-0x2534	RB14	R	
0x2538-0x257C	RB15	R	
Acceptance Filter Mask Registers			
0x2F00	RB0_AMR	R/W	RX Buffer 0 Acceptance Filter Mask Register
0x2F04	RB1_AMR	R/W	RX Buffer 1 Acceptance Filter Mask Register
0x2F08	RB2_AMR	R/W	RX Buffer 2 Acceptance Filter Mask Register
0x2F0C	RB3_AMR	R/W	RX Buffer 3 Acceptance Filter Mask Register

0x2F10	RB4_AMR	R/W	RX Buffer 4 Acceptance Filter Mask Register
0x2F14	RB5_AMR	R/W	RX Buffer 5 Acceptance Filter Mask Register
0x2F18	RB6_AMR	R/W	RX Buffer 6 Acceptance Filter Mask Register
0x2F1C	RB7_AMR	R/W	RX Buffer 7 Acceptance Filter Mask Register
0x2F20 - 0x2F54	RB8_AMR- RB15_AMR	R/W	RX Buffer 8 to RX Buffer 15 Acceptance Mask Registers (The number of RX Buffer Acceptance Mask Registers depends on the number of RX buffers used.)

RX Message Register (Mailbox) Description

1. RX Message ID Register

Table 28. RX Message ID Register Description

Bits	Name	Access	Reset Value	Description
31:21	BID	R	0	Standard Message ID. The base ID (11 bits) of the received message. This field is valid for both standard and extended frame formats of CAN and CAN FD.
20	SRR	R	0	Substitute Remote Transmission Request. 1: Indicates the received message is a Remote Frame in CAN Base Format. 0: Indicates the received message is Data Frame in CAN Base Format.
19	IDE	R	0	Identifier Extension 1: Indicates the received message frame is in Extended Format. 0: Indicates the received message frame is in Base Format.
18:1	EXID	R	0	Extended ID The extended identifier(18 bits) of the received message frame. This field is valid only for Extended Format Frames of CAN and CAN FD.
0	RTR	R	0	Remote Transmission Request 1: Indicates the received message is a Remote Frame in

				CAN Extended Format. 0: Indicates the received message is Data Frame of CAN Base Format.
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2. RX Message DLC Register

Table 29. RX Message DLC Register Description

Bits	Name	Access	Reset Value	Description
31:28	DLC	R	0	Data Length Code. Indicates the data length code of the control field of the received CAN and CAN FD message frame. The value is in the number of bytes.
27	EDL/FDF	R	0	Extended Data Length/FD Frame Format 1: Indicates CAN FD message frame was received. 0: Indicates the CAN message frame was received.
26	BRS	R	0	Bit Rate Switch This bit indicates whether the core had switched the bit rate while receiving the message frame. 1: The data field of the frame was received at a data bit rate. 0: The data field of the frame was received at a nominal bit rate.
25:0	Reserved	-	0	Reserved

3. RX Message Data Word 0 (DW0) Register

Table 30. RX Message Data Word Register Description

Bits	Name	Access	Reset Value	Description
31:24	DB0	R	0	Data Byte 0
23:16	DB1	R	0	Data Byte 1
15:8	DB2	R	0	Data Byte 2
7:0	DB3	R	0	Data Byte 3

4. Acceptance Mask Register(RB*_AMR)

Table 31. Acceptance Filter Mask Register Description

Bits	Name	Access	Reset Value	Description
31:21	BID	R	0	Standard Message ID Mask Register These bits are used for masking the Base Identifier in a Standard Frame. 1: Indicates the corresponding bit in the Acceptance Code Register(BID_ACR) is used when comparing the incoming message base identifier. 0: Indicates the corresponding bit in Acceptance Code Register (BID_ACR) is not used when comparing the incoming message base identifier
20	SRR	R	0	Substitute Remote Transmission Request.Mask Register This bit is used for masking RTR in standard frames. 1: Indicates the corresponding bit in the Acceptance Code Register(SRR_ACR) is used when comparing the incoming message SRR. 0: Indicates the corresponding bit in the Acceptance Code Register(SRR_ACR) is not used when comparing the incoming message SRR bit.
19	IDE	R	0	Identifier Extension Mask Register This bit is used for masking the IDE bit. 1: Indicates the corresponding bit in the Acceptance Code Register(IDE_ACR) is used when comparing the incoming message IDE bit. 0: Indicates the corresponding bit in the Acceptance Code Register(IDE_ACR) is not used when comparing the incoming message IDE bit.
18:1	EXID	R	0	Extended ID Mask Register These bits are used for masking the Extended Identifier in a Standard Frame. 1: Indicates the corresponding bit in the Acceptance Code Register(EXID_ACR) is used when comparing the incoming message extended identifier. 0: Indicates the corresponding bit in the Acceptance Code Register(EXID_ACR) is not used when comparing the incoming message extended identifier.
0	RTR	R	0	Remote Transmission Request

				<p>This bit is used for masking RTR in extended frames.</p> <p>1 : Indicates the corresponding bit in the Acceptance Code Register(RTR_ACR) is used when comparing the incoming message RTR bit.</p> <p>0: Indicates the corresponding bit in the Acceptance Code Register (RTR_ACR) is not used when comparing the incoming message RTR bit.</p>
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Resource Utilization

The FPGA resources consumed by the CAN FD controller core are summarized as follows;

Table 32. Resource Utilization by CAN FD controller core

Board	ZYNQ-7 ZC706 Evaluation Board		
Device	xc7z045ffg900-2		
Vivado Version	2021.1		
Resource Utilization			
Site Type	Available	Utilization	Utilization %
LUT	218600	3590	1.64
FF	437200	3105	0.71
DSP	900	0	0
BRAM36	545	1	0.18
BRAM18	1090	16	1.46

***Note:** The resource utilization report is based on the CAN FD Core configured to 32 TX mailboxes and 16 RX mailboxes.

Clocking and Reset

Clock

The CAN FD IP includes two clocks: the CAN FD clock and the AXI4-lite clock. These clocks can either be synchronous or asynchronous with one another. When they are asynchronous, the AXI4-lite clock must operate at a higher frequency than the CAN FD clock.

The CAN FD clock frequency can be 8 to 80 MHz.

Reset

The CAN FD IP can be reset using either the system (hard) reset input port or a software-controlled reset. Both methods completely reset the entire CAN FD core.

Example Design

Overview

This section provides the example design with the core. This example design consists of a synthesizable design.

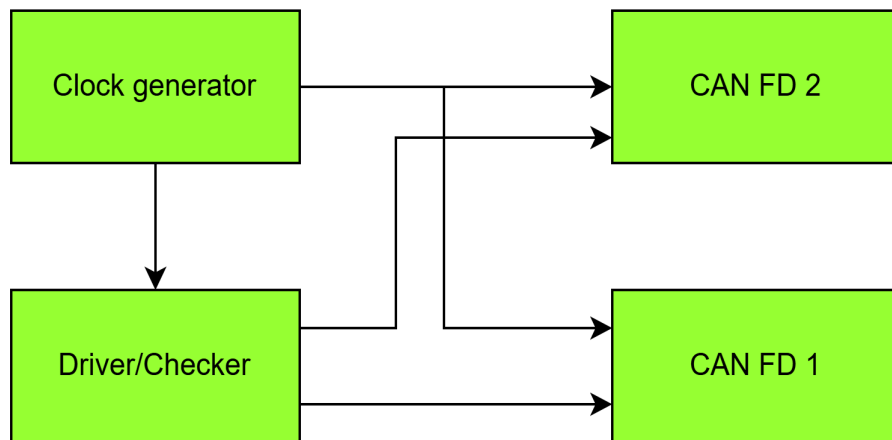


Figure 2. Example Design

The design includes the following modules

- Clock generator
The clocking wizard is used to generate a clock for the CAN FD clock and AXI clock.
- Driver/Checker
An AXI traffic generator in system test mode is used to configure and program CAN FD IP.
- CAN FD IP
Two CAN FD IPs (CAN FD 1 and CAN FD 2) are used, both are configured to transmit and receive the packets.

Simulating the Example Design

Example Sequence

The testbench performs the following tasks:

- Writes SRR to reset the CAN FD IP core.
- Writes the Baud Rate Prescaler and Bit Timing Registers for Nominal Bit Rate in CAN FD 1 and CAN FD 2.
- Writes the Baud Rate Prescaler and Bit Timing Registers for Data Bit Rate in CAN FD 1 and CAN FD 2.
- Programs ID Filter and Mask registers in CAN FD 1 and CAN FD 2.
- Configures both nodes to operate in Normal Mode.
- Programs Interrupt Enable Register to enable interrupt generation.
- The SRR is programmed to enable the CEN bit, which enables the CAN FD core
- Writes Messages in TX buffers of CAN FD 1; ID register, DLC register, and Data words (data is transmitted according to value at DLC register).
- Writes Messages in TX buffers of CAN FD 2; ID, DLC, and Data words (data is transmitted according to value at DLC register)
- Write TRR in both CAN FD 1 and CAN FD 2 to request the buffers are ready for transmission.

Example Configuration

- AXI clock: *100 MHz*
- CAN clock: *40 MHz*
- Nominal Bit Rate: *625 Kb/s*
- Baud Rate Prescaler : *4*
- Time Segment 1: *12 time quanta*
- Time Segment 2: *3 time quanta*
- Synchronization Jump Width: *3-time quanta*
- Sample point at: *80%*
- Data Phase Bit Rate: *5 Mbps*
- Data Phase Baud Rate Prescaler : *1*
- Data Phase Time Segment 1: *5 time quanta*
- Data Phase Time Segment 2: *2 time quanta*
- Data Phase Synchronization Jump Width: *2 time quanta*
- Sample point at: *60%*

Testbench

The figure below shows the testbench for the CAN example design.

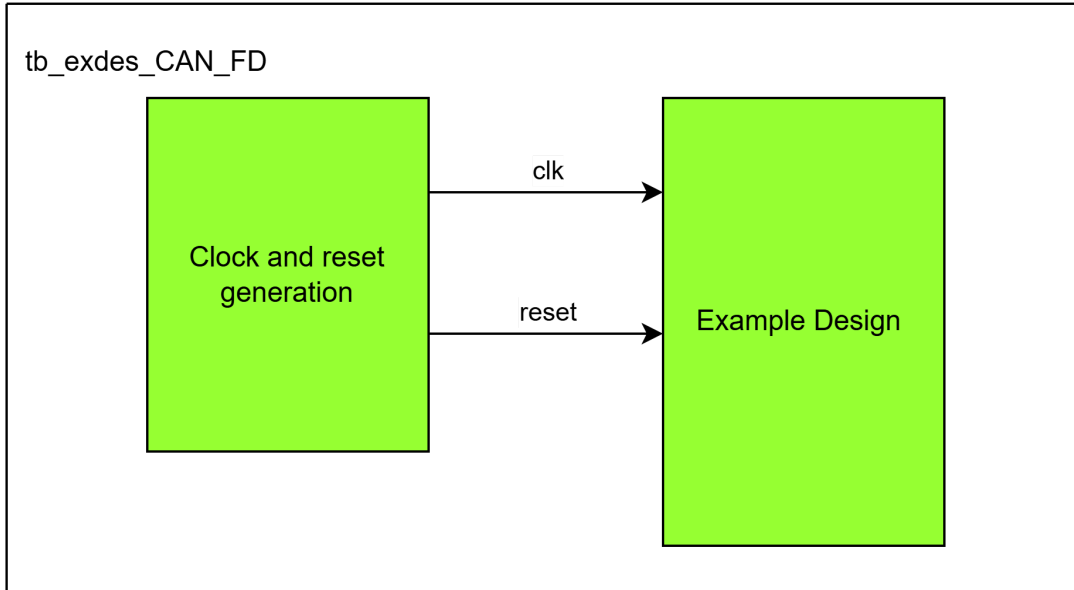


Figure 3. CAN FD Example Design Testbench

Synthesizable Design

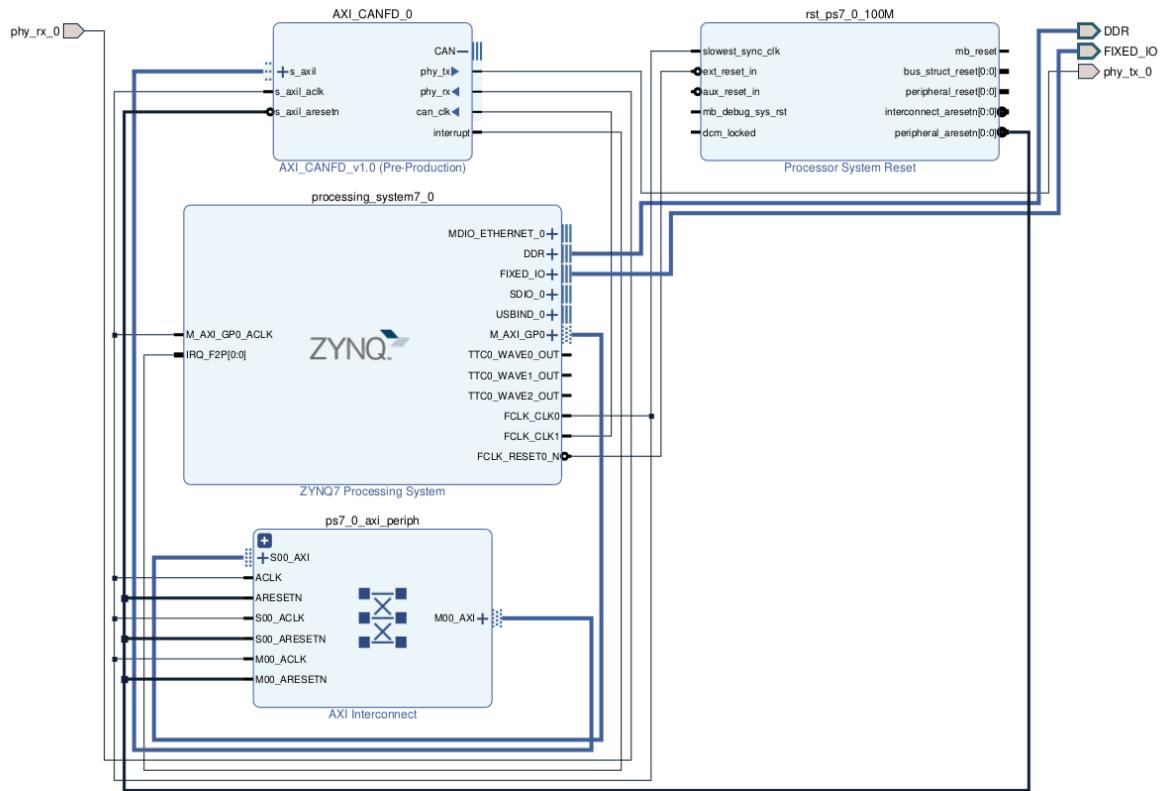


Figure 4. Synthesizable CAN FD Design

The synthesizable example design is shown in the above picture.

Note: This example design is created for the Zybo (xc7z010c1g400-1) board.

In this design, ZYNQ7 Processing System is used as a host processor. Therefore, a software application is required to run this design. The CAN FD IP core is interfaced with the Processing System by AXI4-Lite interface. The TX and Rx lines of the CAN interface are mapped to external ports and clocks are provided from the host processor. (The IP has two clocks; AXI and CAN clocks). In the SDK part, the CAN FD core has to be initialized and configured with the initial parameters such as Baud Rate Prescalers, Bit Timings, operation mode selection, interrupt enable, Acceptance filter IDs and Masks.

References

1. Robert, Bosch. *CAN with Flexible Data-Rate*. 70839, Gerlingen, Germany, 2012.
2. (“ISO 11898-1:2015 - Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signaling”)]
3. Vivado AXI Reference Guide ([UG1037](#))
4. “CAN with Flexible Data Rate (CAN FD).” AMD, ([Link](#))

Revision History

The following table shows the revision history of this product guide - PGL202.

Table 33. IP core Revision History

Date	Version	Detail
November 21, 2024	1.0	<ul style="list-style-type: none"> • Initial Release.
December 11, 2024	2.0	<ul style="list-style-type: none"> • Shifted previous verilog wrapper based design into Vivado IP Integrator-based design with Bare Metal Application verification method. • Added information about synthesizable design.

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications including ADAS, Surveillance, Computer Vision, FinTech, etc.

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