Introduction

A JPEG XS IP core is a hardware solution for real-time, visually lossless image and video compression, designed for applications requiring low latency, high-quality video, and minimal resource usage. It consists of an AXI4-Lite interface, which allows easy IP control.

Features

- Compliant with ISO/IEC 21122-1
- AXI4-Lite control interface
- AXI4-Stream data interfaces
- Color space RGB, YCbCr
- Color Sampling 4:4:4, 4:2:2
- Fixed latency - four lines of pixels
- Programmable compression rate
- Single and dual pixel per clock architectures

Applications

- FPGA-based Imaging systems
- Live production, broadcast
- Automotive Cameras/ ADAS Systems
- Sensor compression

IP FACTS	
Core Specs	
Supported Device Family	Xilinx's 7 Series, Zynq-7000
Supported User Interfaces	AXI4-Lite
Resources Utilization	Included in this document
Provided Sources	
Documentation	Product Guide
Design Files	Not Provided
Example Design	Yes
Test Bench	Not Provided
Simulation Models	Not Provided
Supported Software Drivers	Standalone
Tested Design Flows	
Design Entry Tools	Xilinx's Vivado Design Suite
Simulation	Xilinx's Vivado Simulator
Synthesis Tools	Xilinx's Vivado Synthesis
Support	
Provided by LogicTronix	

Table 1. IP Facts

For IP Support and Interest: sales@logictronix.com or info@logictronix.com

Overview

JPEG XS IP Description

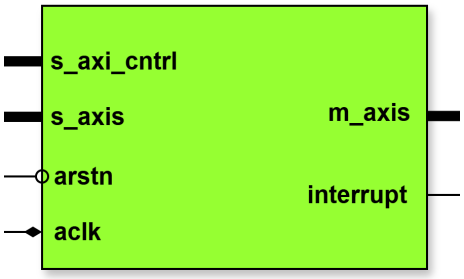

Figure 1. JPEG Encoder IP Top-Level View

The IP core has configuration registers for setting image resolution, image quality and bitrate control parameters; quantization and refinement parameters of the compressed image and enabling/disabling interrupts. The registers are accessed via AXI4-Lite interface. The core starts up in Configuration Mode and starts encoding images in Normal Mode.

The IP core allows configuring Image Resolution Register and Quantization and Refinement Register at run time so that images of different resolutions and quality factors can be encoded. However the configuration should be done only in configuration more

Port Description

. The JPEG XS encoder core ports are described by the following interfaces.

1. Clock and Reset signal Interface

These signals are summarized in the following table.

Table 2. Clock, Reset Signal Interface Description

Signal Name	Width	Direction	Description
aclk	1	IN	Core clock
arstn	1	IN	Core synchronous active low reset
interrupt	1	OUT	Core Interrupt line

2. Data Interface

The IP has only two data interfaces that implement the AXI4-Stream interface protocol. The Slave interface is used to provide pixel data into IP and the master interface is used to get the data out of the IP. For more information, visit **UG761**.

AXI4-Stream Signals

The following table gives a short description of the individual signal pins of the AXI4-Stream Interface.

Table 3. AXI4-Stream Master Interface Signal Names and Descriptions

Signal Name	Width	Direction	Description
m_axis_tdata	32	OUT	Output Encoded Data
m_axis_tvalid	1	OUT	Indicates the IP is driving a valid transfer
m_axis_tready	1	IN	Indicates receiver is ready to accept transfer
m_axis_tlast	1	OUT	Indicates boundary of a packet
m_axis_tstrb	1	OUT	Output data strobe indicates whether the content of the associated byte of tdata is processed as a data byte or position byte

Table 4. AXI4-Stream Slave Interface Signal Names and Descriptions

Signal Name	Width	Direction	Description
s_axis_tdata	24/48	IN	Input pixel data
s_axis_tvalid	1	IN	Indicates the transmitter is driving a valid transfer
s_axis_tready	1	OUT	Indicates the IP is ready to accept transfer
s_axis_tlast	1	IN	Indicates boundary of a packet
s_axis_tstrb	4	IN	indicates whether the content of the associated byte of tdata is processed as a data byte or position byte

3. Control Interface

The IP consists of an AXI4-Lite interface as a control interface. This allows us to configure or control the IP dynamically. This interface will be connected to Zynq PS or Microblaze.

AXI4-Lite Interface Signals

The AXI4-Lite Interface signal names and their description are given in the following table.

Table 5. AXI4-Lite Interface Signal Names and Description

Signal Name	Width	Direction	Description
s_axi_lite_awvalid	1	IN	AXI4-Lite Write Address Channel Write Address Valid
s_axi_lite_awread	1	OUT	AXI4-Lite Write Address Channel Write Address Ready.
s_axi_lite_awaddr	7	IN	AXI4-Lite Write Address Bus
s_axi_lite_wvalid	1	IN	AXI4-Lite Write Data Channel Write Data Valid
s_axi_lite_wready	1	OUT	AXI4-Lite Write Data Channel write Data Ready.
s_axi_lite_wdata	32	IN	AXI4-Lite Write Data bus
s_axi_lite_wstrb	4	IN	AXI4-Lite Write Data Strobe
s_axi_lite_bresp	2	OUT	AXI4-Lite Write Response Channel.
s_axi_lite_bvalid	1	OUT	AXI4-Lite Write Response Channel Response Valid.
s_axi_lite_bready	1	IN	AXI4-Lite Write Response Channel Ready.
s_axi_lite_arvalid	1	IN	AXI4-Lite Read Address Channel Read Address Valid
s_axi_lite_arready	1	OUT	AXI4-Lite Ready.
s_axi_lite_araddr	7	IN	AXI4-Lite Read Address Bus
s_axi_lite_rvalid	1	OUT	AXI4-Lite Read Data Channel Read Data Valid
s_axi_lite_rready	1	IN	AXI4-Lite Read Data Channel Read Data Ready.
s_axi_lite_rdata	32	OUT	AXI4-Lite Ready Data Bus.

s_axi_lite_rresp	2	OUT	AXI4-Lite Read Response Channel Response.

Register Space

The IP has specific registers so that IP parameters can be set by accessing these registers and then setting the appropriate hex value. The register can be accessed by its offset address. These registers are programmed by AXI4-Lite Interface.

JPEG IP Register Address Map

Table 6. JPEG IP Register Address Map

Address offset	Register Name	Access	Description
0x00	SRR	R/W	Software Reset Register
0x04	MSR	R/W	Mode Select Register
0x08	MRSR	R	Maximum Resolution Status Register
0x0C	IRR	R/W	Image Resolution Register
0x10	QRR	R/W	Quantization and Refinement Parameter Register
0x014	SR	R	Status Register
0x018	ISR	R	Interrupt Status Register
0x01C	IER	R/W	Interrupt Enable Register
0x020	ICR	W	Interrupt Clear Register

Register Description

1. Software Reset Register(SRR); 0x000

Table 7. Software Reset Register Description

Bits	Name	Access	Reset Value	Description
31:2	Reserved	-	0	Reserved
1	JXSEN	R/W	0	JPEG XS Enable 1: Enable JPEG XS Core 0: Disable JPEG XS Core
0	SRST	R/W	0	Reset

				1: resets core Writing 1 to this bit resets the entire JPEG XS core including SRR

2. Mode Select Register(MSR); 0x004

Table 8. Mode Select Register Description

Bits	Name	Access	Reset Value	Description
31:0	Reserved	-	0	Reserved

3. Maximum Resolution Status Register; 0x08

Table 9. Maximum Resolution Status Register Description

Bits	Name	Access	Reset Value	Description
31:16	MAX_IH	R	Parameterized Image Resolution	Maximum Image Height
15:0	MAX_IW	R		Maximum Image Width

4. Image Resolution Register; 0x0C

Table 10. Image Resolution Register Description

Bits	Name	Access	Reset Value	Description
31:16	IH	R/W	0	Image Height
15:0	IW	R/W		Image Width

5. Quantization and Refinement Parameter Register; 0x10

Table 11. Quantization and Refinement Parameter Register Description

Bits	Name	Access	Reset Value	Description
31:16	Reserved	-	0	Reserved
15:8	Qp	R/W	0	Quantization
7:0	Rp	R/W	0	Refinement

6. Status Register; 0x14

Table 12. Status Register Description

Bits	Name	Access	Reset Value	Description
31:3	Reserved	-	0	Reserved
2	EN_DONE	R	0	Encode done Indicates the completion of encoding one frame.
1	IDLE_S	R	0	Idle Status Indicates the current state of the core . 1: The core is in Idle state. 0: The core is in Encoding state..
0	CONFIG_S	R	1	Configuration Mode Status Indicates the current mode of the core. 1: The core is in configuration mode. 0: The core is not in configuration mode and is ready to encode.

7. Interrupt Status Register; 0x18

Table 13. Interrupt Status Register Description

Bits	Name	Access	Reset Value	Description
2	E_DONE	R	0	Encoding Done : Indicates encoding of the current image is complete.
1	C_READY	R	0	Core Ready : Indicates Core is ready for encoding.
0	RCONFIG_ ERR	R	0	Resolution Configuration Error: Indicates the resolution programmed to the core is invalid (does not lie within range). (The maximum resolution that can be programmed is the resolution set from the Customization Parameter).

8. Interrupt Enable Register; 0x1C

Table 14. Interrupt Enable Register Description

Bits	Name	Access	Reset Value	Description
2	E_DONE_EN	R/W	0	Encoding Done Interrupt Enable 1: Enables interrupt generation if E_DONE bit in ISR is set. 0: Disables interrupt generation if E_DONE bit in ISR is set.
1	C_READY_EN	R/W	0	Core Ready Interrupt Enable 1: Enables interrupt generation if C_READY bit in ISR is set. 0: Disables interrupt generation if C_READY bit in ISR is set.
0	RCONFIG_ERR_EN	R/W	0	Resolution Configuration Error Interrupt Enable 1: Enables interrupt generation if RCONFIG_ERR bit in ISR is set. 0: Disables interrupt generation if RCONFIG_ERR bit in ISR is set.

9. Interrupt Clear Register; 0x20

Table 15. Interrupt Enable Register Description

Bits	Name	Access	Reset Value	Description
2	E_DONE_C	W	0	Encoding Done Interrupt Clear 1: Clears Encoding Done Interrupt status bit.
1	C_READY_C	W	0	CoreReady Interrupt Clear 1: Clears Core Ready Interrupt status bit.
0	RCONFIG_ERR_C	W	0	Resolution Configuration Error Interrupt Clear 1: Clears Resolution Configuration Error Interrupt status bit..

Resource Utilization

The FPGA resources consumed by the JPEG XS Encoder IP is summarized as follows;

Table 16. Resource Utilization by JPEG XS Encoder IP with one sample per clock encoding design

Board	ZedBoard Zynq Evaluation and Development Kit		
Device	xc7z020clg484-1		
Vivado Version	2021.1		
Resource Utilization			
Site Type	**Available**	**Utilization**	**Utilization %**
LUT	53200	10517	19.77
FF	106400	13845	13.01
DSP	220	0	0
BRAM	140	.28	20.00

Table 17. Resource Utilization by JPEG XS Encoder IP for two sample per clock encoding design

Board	ZedBoard Zynq Evaluation and Development Kit		
Device	xc7z020clg484-1		
Vivado Version	2021.1		
Resource Utilization			
Site Type	**Available**	**Utilization**	**Utilization %**
LUT	53200	14207	26.70
FF	106400	15914	14.96
DSP	220	0	0
BRAM	140	.29.5	21.07

Note: This resource utilization report is based on resolution of 1920x1080 image at clock frequency 200 MHz. The resource can vary on different resolutions and different clocks.

Clocking

The JPEG XS IP has one system clock. Data interface, control interface and core encoder works on the same clock.

Resets

The JPEG XS IP can be reset using either the system (hard) reset input port or a software-controlled reset. Both methods completely reset the entire JPEG XS core

Example Design

This section provides an example design of the core. This example design only consists of a synthesizable design.

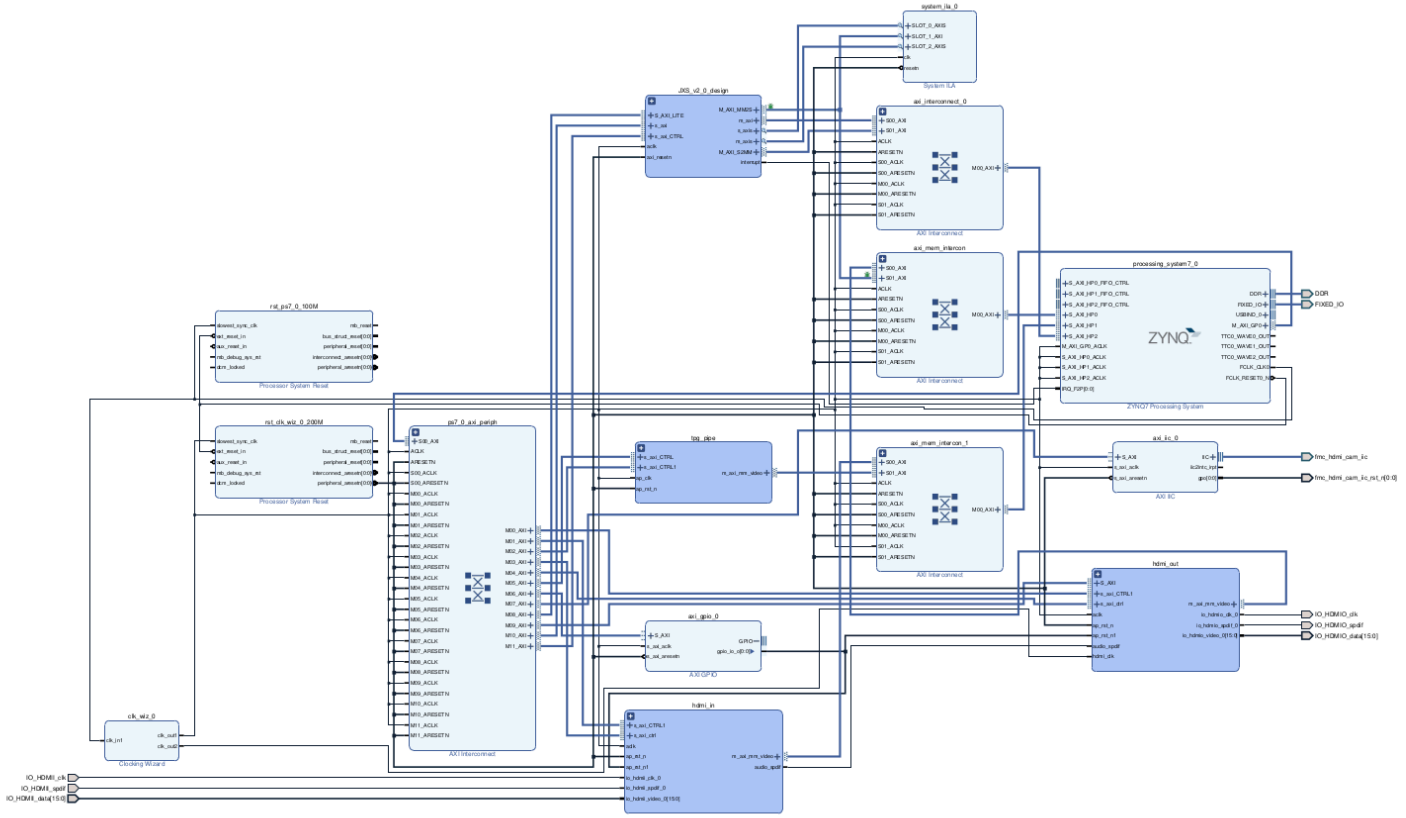

Figure 2. Synthesizable JPEG XS IP core design

The synthesizable example design is shown in the above picture.

In this design, the HDMI input video data is first captured and then encoded using a JPEG XS IP core. To manage the flow of high-bandwidth video data, an AXI Video Direct Memory Access (VDMA) module is employed to temporarily buffer the incoming HDMI video frames. The VDMA stores these frames in memory before they are passed on to the Encoder.

The JPEG IP receives the buffered video frames through an AXI4-Stream interface. After encoding the video data, the IP writes the resulting compressed output to memory using an AXI4 Memory-Mapped interface. This allows for efficient storage and further processing of the encoded data.

The memory addresses used for these AXI4 Memory-Mapped transactions are configured via an AXI4-Lite interface.

References

1. "JPEG - JPEG XS." *Jpeg.org*, jpeg.org/jpegxs/..
2. Vivado AXI Reference Guide (UG1037).
3. Vivado Design Suite User Guide: Designing with IP (UG896).

Revision History

The following table shows the revision history of this product guide, PGL010.

Table 17. IP core Revision History

Date	Version	Detail
August 15, 2025	1.0	Initial Release

About LogicTronix

LogicTronix provides Turnkey Solutions, Design Services, and Intellectual Property (IP) to customers on FPGA Design, Computer/Machine Vision, Machine Learning Acceleration on FPGA [Edge or Cloud] for various applications, including ADAS, Surveillance, Computer Vision, FinTech, etc.

LogicTronix also offers solutions on "Real-Time Traffic Video Analytics Solution (TVAS) - including Automatic vehicle Number-Plate Recognition (ANPR) Solution", "Enhancing Financial Trading Algorithms with AI/ML," and "High-Frequency Trading (HFT) based Infrastructure".

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